Flyback Converter

Project report submitted in partial fulfillment of the requirements of

Bachelor of Technology

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1 Introduction

Flyback converter (Figure 1) is a dc-dc converter topology derived from buck-boost converter (Figure 2) with inductor split up to form a transformer for galvanic isolation between input and output. Section 1.1 describes the working of buck-boost converter followed by description of flyback converter in Section 1.2.

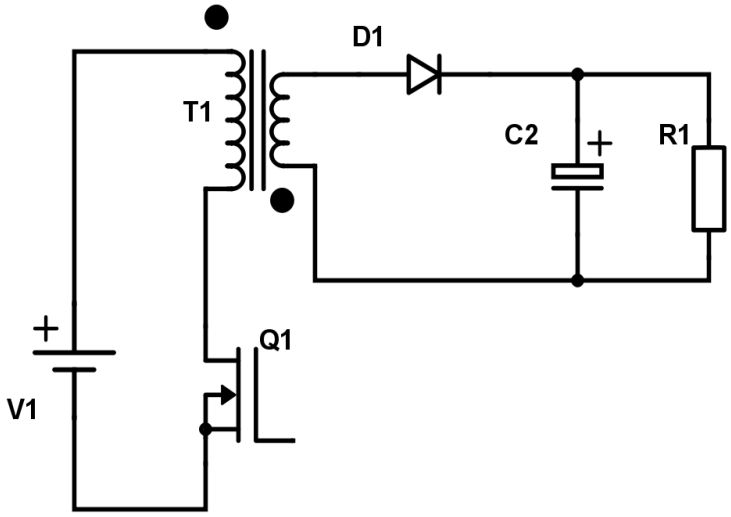

Figure 1: Flyback converter

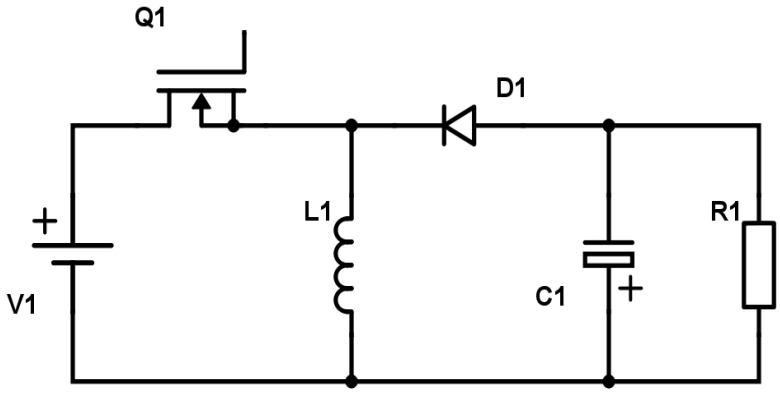

Figure 2: Buck-Boost converter

1.1 Buck-Boost converter

A buck-boost converter has an output voltage that is either greater than or less than input voltage depending on duty cycle of switching pulse. Its voltage gain expression is given by

$$\frac{V_{out}}{V_{in}} = \frac{D}{1-D}$$

V_{out}: $Output\ voltage\ across\ capacitor\ C1$

V_{in}: $Input\ source\ voltage\ V1$

D: $duty\ cycle\ of\ switching\ pulse$

1.1.1 Principle of operation

Let us assume that buck-boost converter is operating in continuous conduction mode (CCM) for analysis. During steady state, voltage V_{out} appears across the capacitor (C1) and a non-zero average current flows through the inductor (L1). The basic operation of buck-boost converter can be understood by analyzing the two states of switch (Q1).

When the switch (Q1) turns ON, input voltage is directly connected to inductor L1, ignoring the on state resistance of switch, and diode D1 gets reverse biased. This leads to rise in current through inductor governed by expression

$$V = L * \left(\frac{di}{dt}\right)$$

$V: Voltage\ across\ inductor$

$L: Value\ of\ inductance$

$i: Inductor\ current$

When the switch (Q1) turns OFF, current through inductor cannot immediately die down to zero, hence, diode (D1) starts conducting due to Faraday's law of electromagnetic induction providing a path for inductor (L1) to charge the output capacitor (C1).

To derive voltage gain expression, we can use the condition that average voltage across inductor should be equal to zero (or else the inductor will burn). During ON state, $V_{L1} = V_{in}$ and during OFF state, $V_{L1} = V_{out}$. Applying average voltage criteria, we get

$$V_{in} * D * T - V_{out} * (1 - D) * T = 0$$

$T: Time\ period\ of\ switching\ pulse$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{D}{1 - D}$$

1.2 Flyback converter

As explained earlier, flyback converter is obtained by replacing inductor with transformer in a buck-boost converter. Corresponding voltage gain expression for flyback converter is

$$\frac{V_{out}}{V_{in}} = \frac{N_2}{N_1} * \frac{D}{1 - D}$$

$N_1: Number\ of\ turns\ on\ the\ primary\ side\ of\ transformer$

$N_2: Number\ of\ turns\ on\ the\ secondary\ side\ of\ transformer$

1.2.1 Principle of operation

We can analyze the two states of switch (Q1) for deriving the voltage gain expression in a manner similar to buck-boost converter.

When the switch Q1 turns ON, input voltage appears across the primary side of transformer, thereby, increasing the energy stored in magnetizing inductance L_m of transformer. Because

of the shown dot polarities in Figure 1, negative voltage appears across the diode D1 and it does not conducts. During this state, capacitor (C1) satiates the current demand of load.

When the switch Q1 turns OFF, current stored in L_m cannot instantaneously die down to zero. Hence, diode (D1) starts conducting because of the Faraday's law of electromagnetic induction and transfer of energy from inductor to output capacitor (C1) takes place.

Figure 3 illustrates the voltage and current waveform for ON and OFF state of switch (Q1). I_p in the plot represents peak value of current through primary side of transformer (T1).

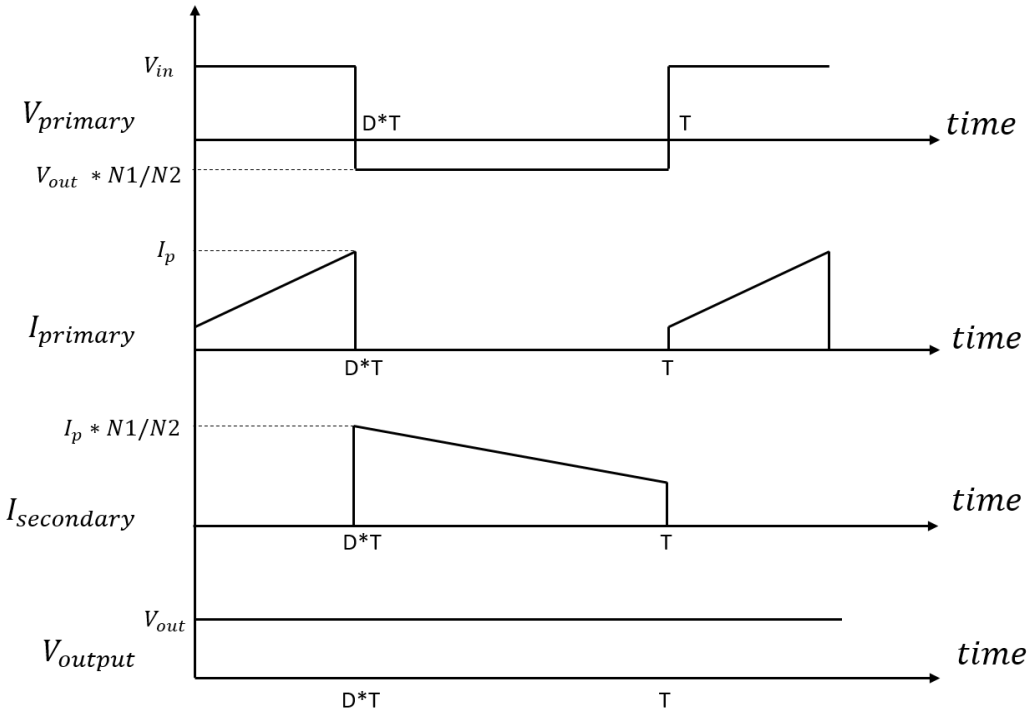

Figure 3: Primary voltage, primary current, secondary current and output voltage waveform for PWM switching of flyback converter

To derive voltage gain expression, we can apply average voltage criteria on the primary side of transformer (T1) to get

$$V_{in} * D * T - V_{out} * \frac{N_1}{N_2} * (1 - D) * T = 0$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{N_2}{N_1} * \frac{D}{1 - D}$$

2 Flyback converter for Modular Multilevel converter

During first part of the project, a flyback converter which takes rectified input from an AC power supply and produces a regulated output voltage was designed as shown in Figure 4. A full bridge rectifier followed by a smoothing capacitor was used to obtain unregulated DC supply for the flyback converter. Further, a transformer with turn ratio of 10:1, designed by *Wurth Electronik,* and TNY279 switch plus controller IC from *Power Integration* was used for galvanic isolation and output regulation respectively. Section 2.1 specifies the rating of flyback

converter followed by functional description and operation of TNY279 in Section 2.2 and Section 2.3 respectively. Design of feedback loop is discussed in Section 2.4 followed by terse description of current limit state machine feature of TNY279 switch in Section 2.5. Toward the end, Section 2.6 and 2.7 covers the schematic of implemented design and its PCB layout in Eagle.

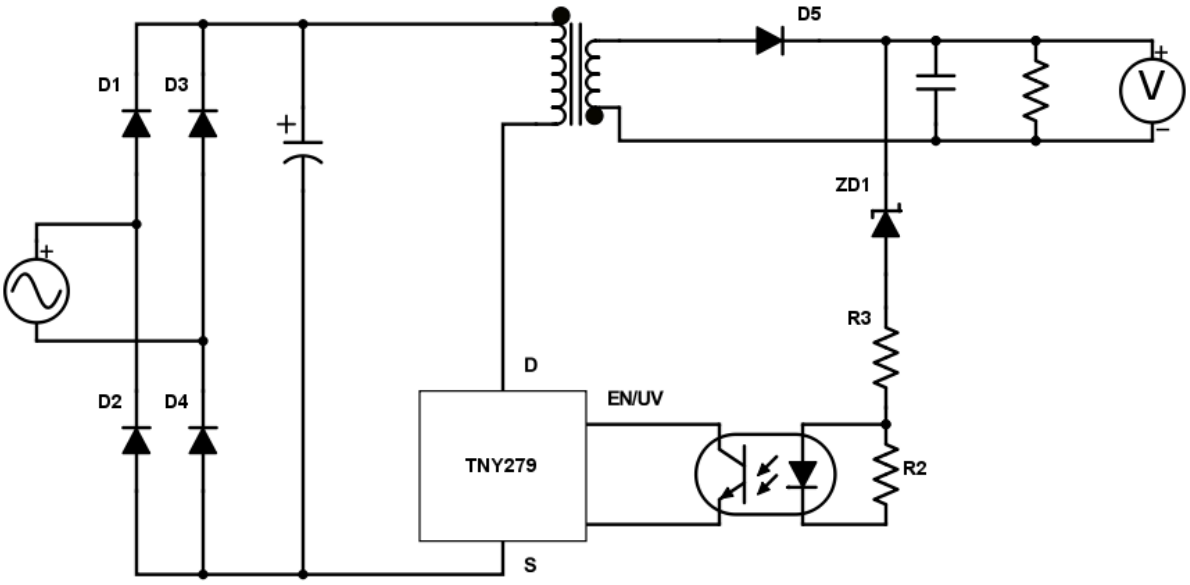

Figure 4: Flyback converter with TNY279 controller IC

2.1 Rating

Input: 85-265 VAC, 3.15 A.

Output: 15 V, 1 A.

2.2 TNY279 Functional description

Figure 5 and Figure 6 shows the package and functional block diagram of TNY279 controller IC used for the design of flyback converter. Pin EN/UV, BP/M, D and S represents enable/under-voltage, bypass/multifunction, drain and source respectively.

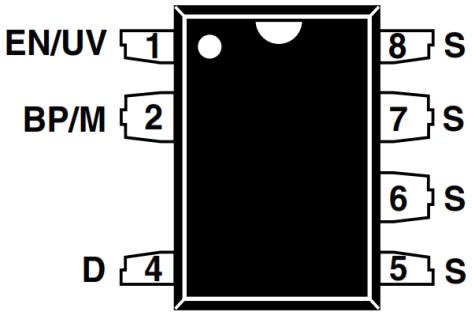

Figure 5: TNY279 package (*Source: Power Integrations*)

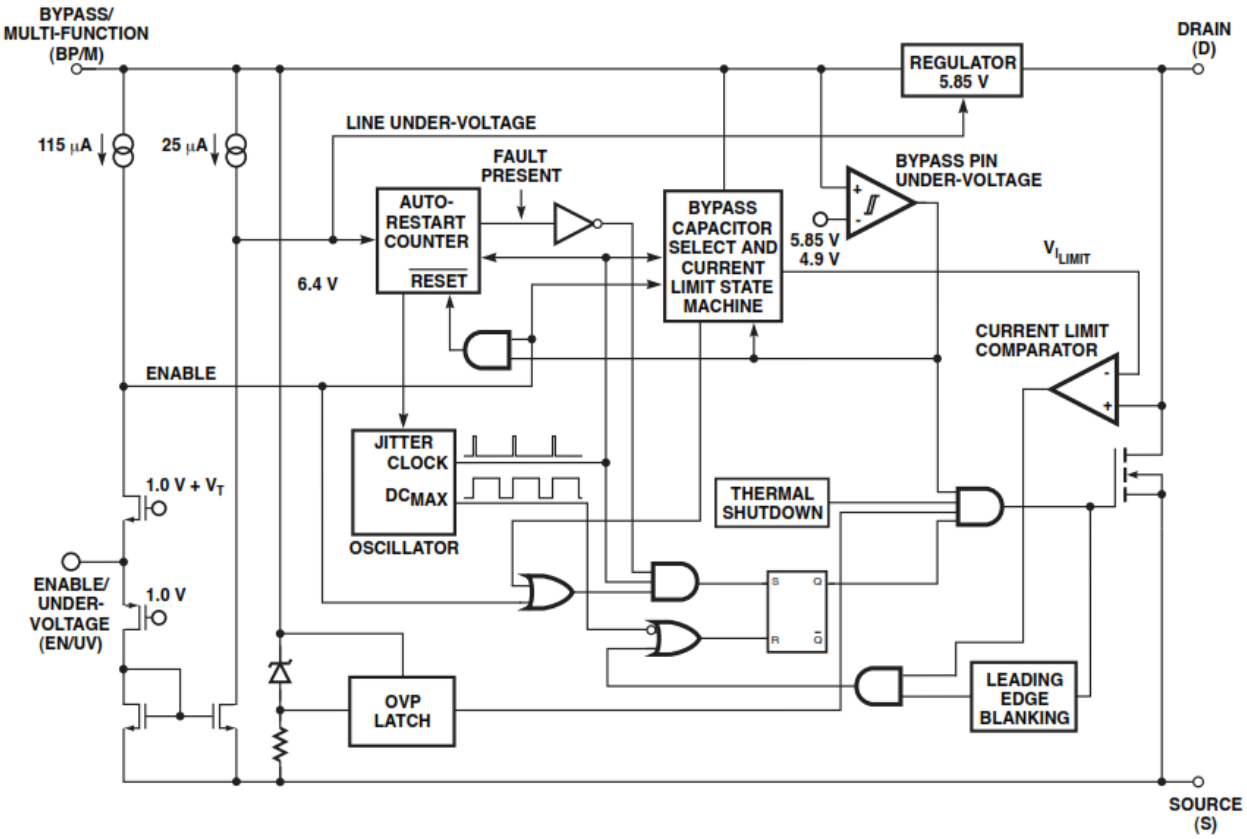

Figure 6: TNY279 functional block diagram (*Source: Power Integrations*)

During ON state, current flows from D to S. BP/M is used to decouple internal power supply and to decide global limiting value of current from drain to source by appropriate choice of capacitor between BP/M and S. An internal current limit state machine adaptively adjusts the local current limit for different loads. EN/UV pin decides the state of switch based on feedback from the output voltage. It can also be used to detect under-voltage on the input side and shut down the MOSFET.

2.3 TNY279 Operation

During normal operation, input circuitry at EN/UV consists of a low impedance source follower set at 1.2 V. If current through this terminal exceeds the threshold value of 115 µA, a logic 1 is generated at the output of this circuitry otherwise a logic 0 is generated. Based on the output of this logic, generated at the rising edge of internally generated 132 kHz signal, state of the switch is controlled. If logic 1 is sampled on the rising edge, MOSFET is turned off otherwise it's turned on. During the cycle when MOSFET is turned on, drain current keeps increasing and MOSFET is turned off as soon as this currents reaches the drain-source current limit as shown in Figure 7. Note that this current limit is updated by current limit state machine based on previous cycles and is explained later.

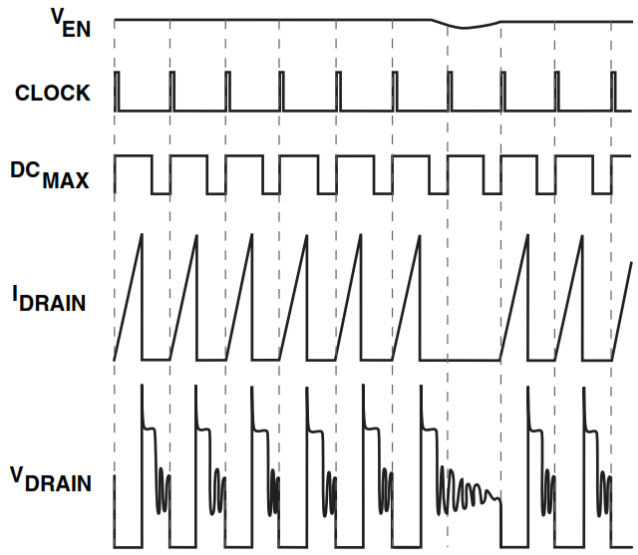

Figure 7: TNY279 switching waveform (*Source: Power Integrations*)

2.4 Feedback circuit

Unlike PWM mode, TNY279 uses on/off method to regulate output voltage using external feedback circuitry. In a typical implementation, reverse breakdown voltage of zener connected in series with optocoupler LED decides the regulated output voltage as shown in Figure 8. When output voltage exceeds the target regulated value, LED starts to conduct and optocoupler pulls the EN/UV pin to zero leading to turning off of switch. To set a regulated output voltage of 15 V, zener diode (ZD1) with reverse breakdown voltage of 15 V was chosen for the design. Resistance (R3) precludes damage to optocoupler by circumscribing the current flowing through LED.

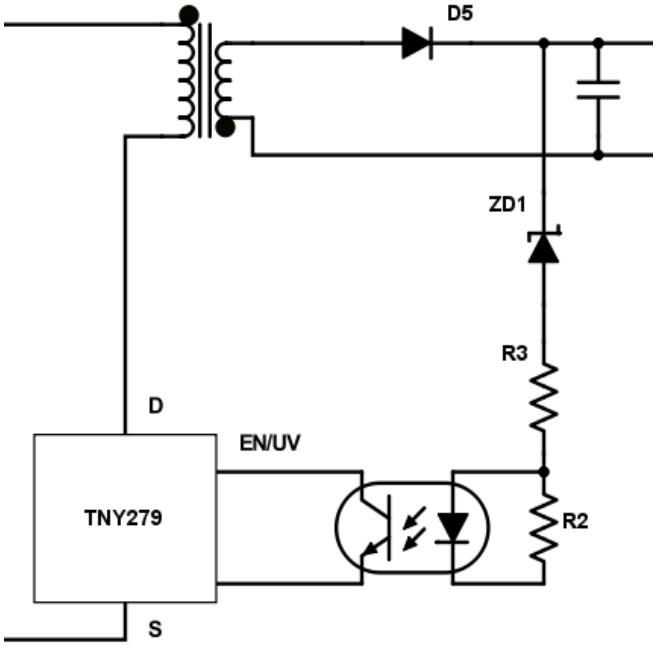

Figure 8: Feedback circuit for TNY279

2.5 Current limit state machine

The current limit state machine reduces the current limit – for comparison with drain current when MOSFET is in on state – when output is connected to light load. This increases the frequency of switching and allays the associated audible noise due to magnetostriction phenomenon in transformer. The state machines observes the past switching cycles of MOSFET to determine the load condition and updates current limit in discrete steps. Figure 9 and Figure 10 represents the state machine adaptation to different load conditions.

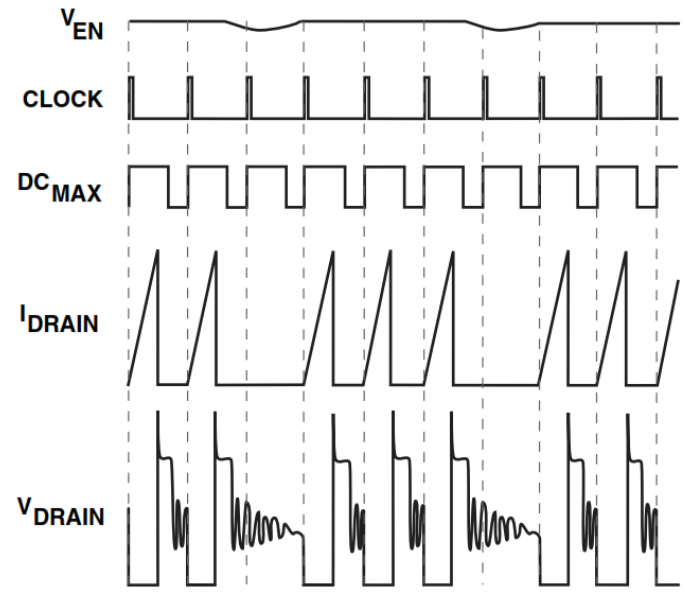

Figure 9: Variation in drain current limit for moderately heavy load (*Source: Power Integrations*)

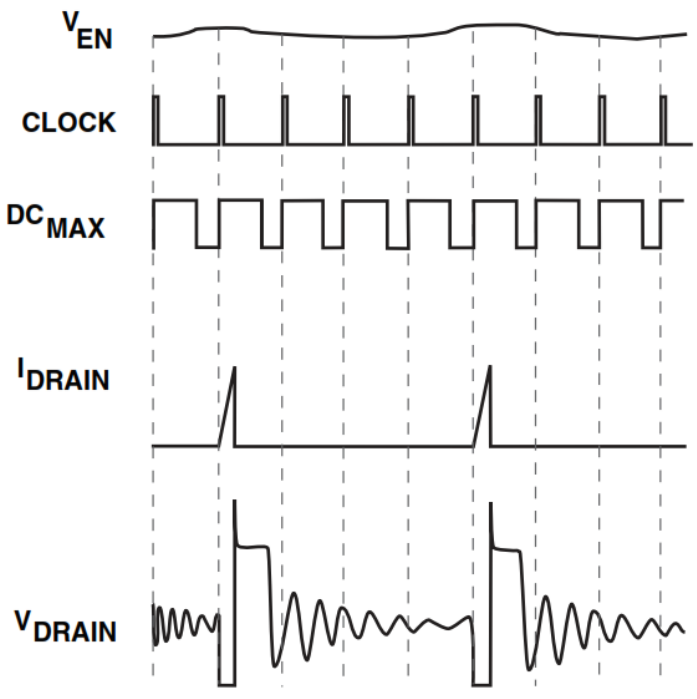

Figure 10: Variation in drain current limit for very light load (*Source: Power Integrations*)

2.6 Schematic

Eagle 7.3 was used to design schematic (Fig. 8) for designed flyback converter.

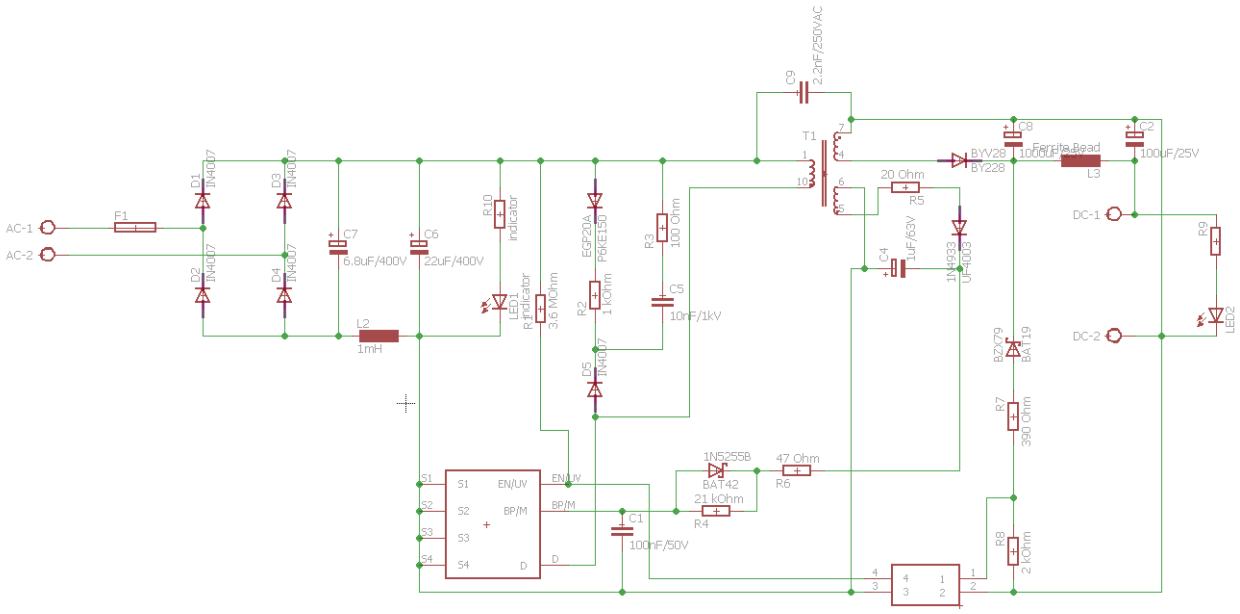

Figure 11: Eagle schematic layout for flyback converter

Overall schematic can be understood by understanding its subparts as illustrated in Figure 12: Full bridge rectifier followed by pi filter - Figure 14. Subpart corresponding to Figure 12 represents a full bridge rectifier followed by pi filter to generate unregulated DC supply. F1, a fuse of rating $3.15\ A$, breaks supply to circuit in the event of a fault. LED1 is meant to indicate on/off state of input. IN4007, with rating of 700 V RMS voltage, was chosen for AC rectification keeping in mind the maximum voltage across diodes.

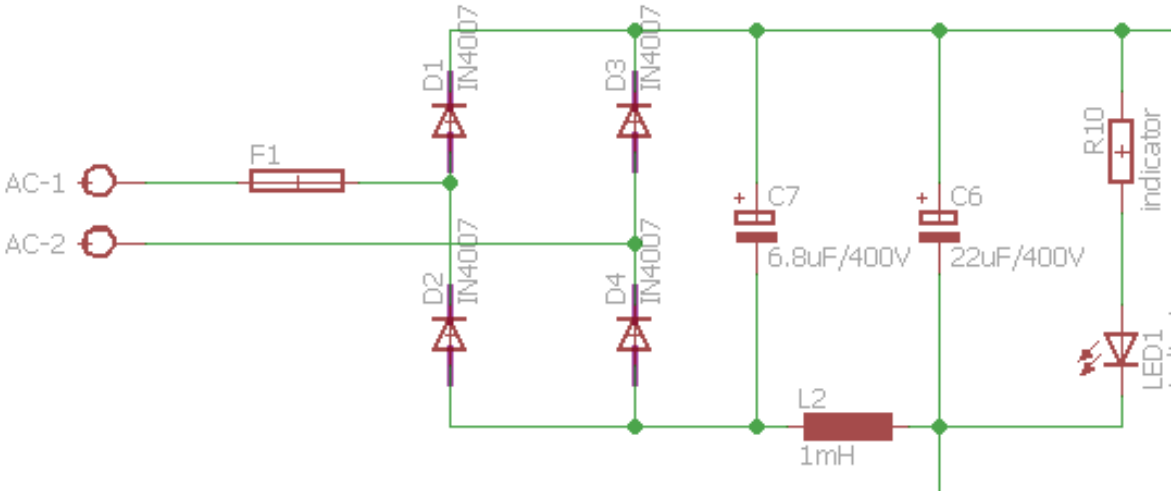

Figure 12: Full bridge rectifier followed by pi filter

Figure 13 represents the snubber circuit on the primary side of transformer to prevent voltage spike, during transition of states. Use of zener clamp and parallel RC optimizes both EMI and energy efficiency.

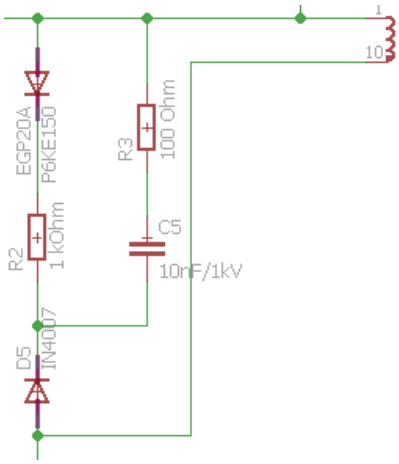

Figure 13: Snubber circuit for primary winding

Remaining subpart of the schematic represents a DC-DC flyback converter topology as shown in Figure 14. Additional circuitry like 3.6 MΩ resistance facilitates under voltage protection; additional bias winding on transformer provides overvoltage protection in the event of open feedback loop faults; indicator LED indicates the state of output.

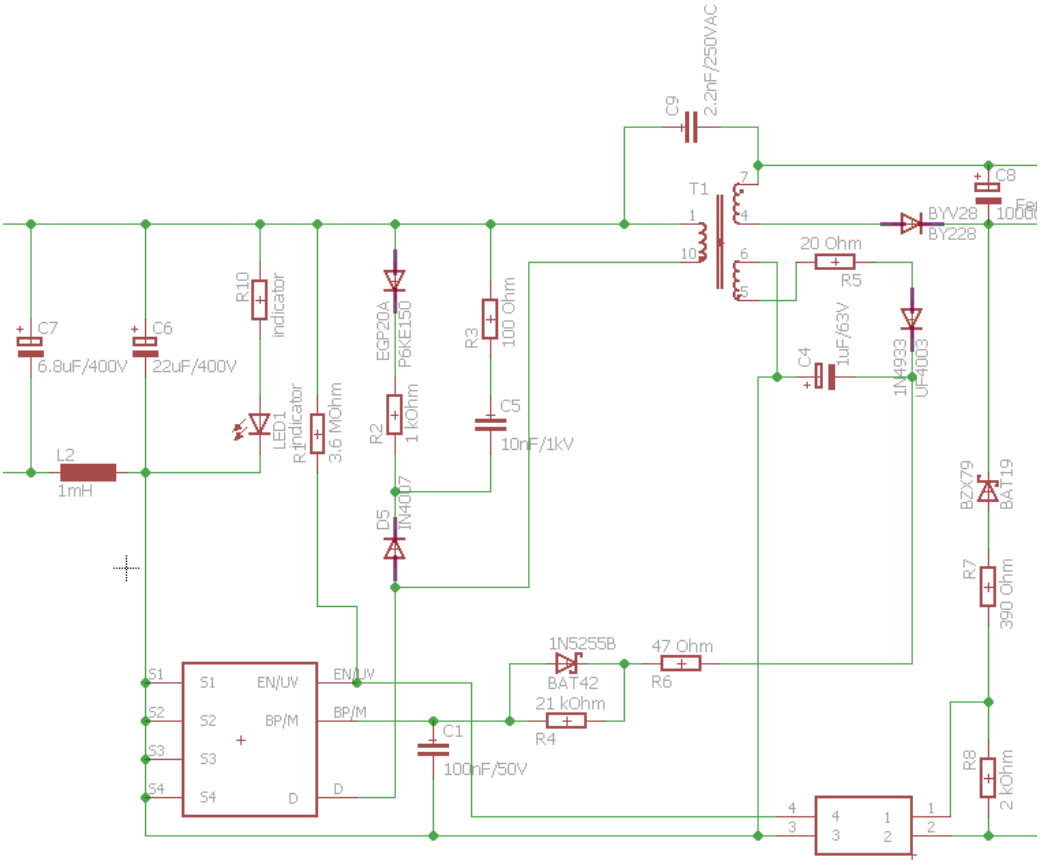

Figure 14: DC-DC flyback converter

In this project, transformer ratio of 10:1 is used for designing a flyback converter with 15 V regulated output and $1\ A$ current rating. Therefore, reverse breakdown voltage of zener diode (in this case 15 V), connected between optocoupler input and output voltage, plus the optocoupler LED forward drop should be such that when the output exceeds 15 V, current should flow in the LED of optocoupler. This would result in current greater than 115 µA to sink from EN/UV pin of TNY279 switch, turning the MOSFET off. Note that transformer ratio of 10:1 was chosen in accordance with zener clamping circuit. As per design criteria of zener clamping circuit, if clamping voltage of zener diode is around 150 V, output voltage of 12 V when reflected on primary would be close to but less than 150 V.

2.7 PCB layout

Eagle 7.3 was used for designing PCB layout as shown in Fig. 12. Basic considerations while designing the layout show in Figure 15 were as follows:

- Minimizing distance between positive and negative terminals of AC source to reduce stray inductance.
- Minimum separation of 2 cm between ground plane of input and output.
- Large distance between input and output connector for safety.

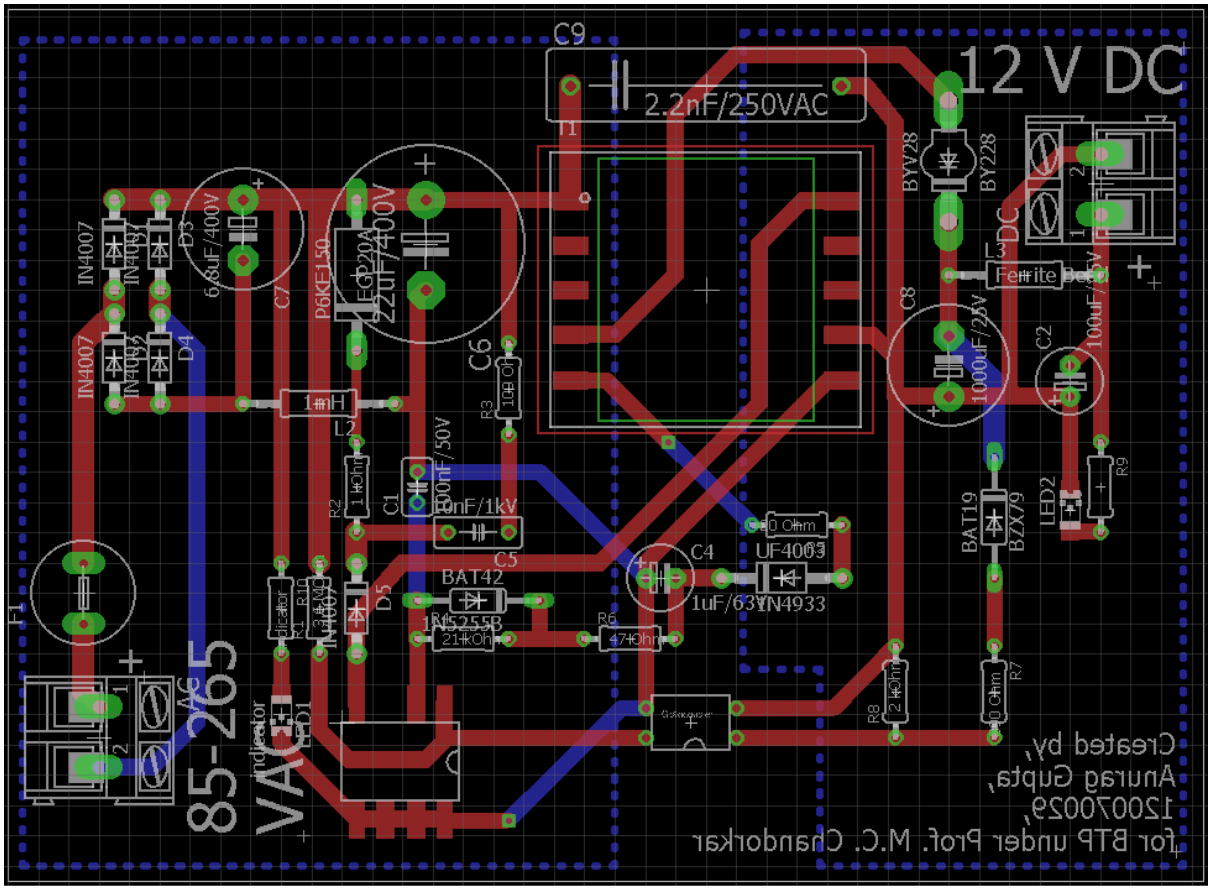

Figure 15: Board layout of the flyback converter

2.8 Testing

In order to characterize output voltage regulation, input voltage sweep from 0 - 230 V (r.m.s) was carried out using variac for resistive load of 16 Ω, 25 Ω, 40 Ω, 55 Ω, 80 Ω, 148 Ω, 200 Ω and no load. Multimeter was used to record input r.m.s voltage and output dc voltage. Error in regulated output voltage is 2% which is within acceptable limit for the application of IGBT gate driver. Figure 16 - Figure 23 shows the plot of output voltage for input voltage sweep with different load conditions.

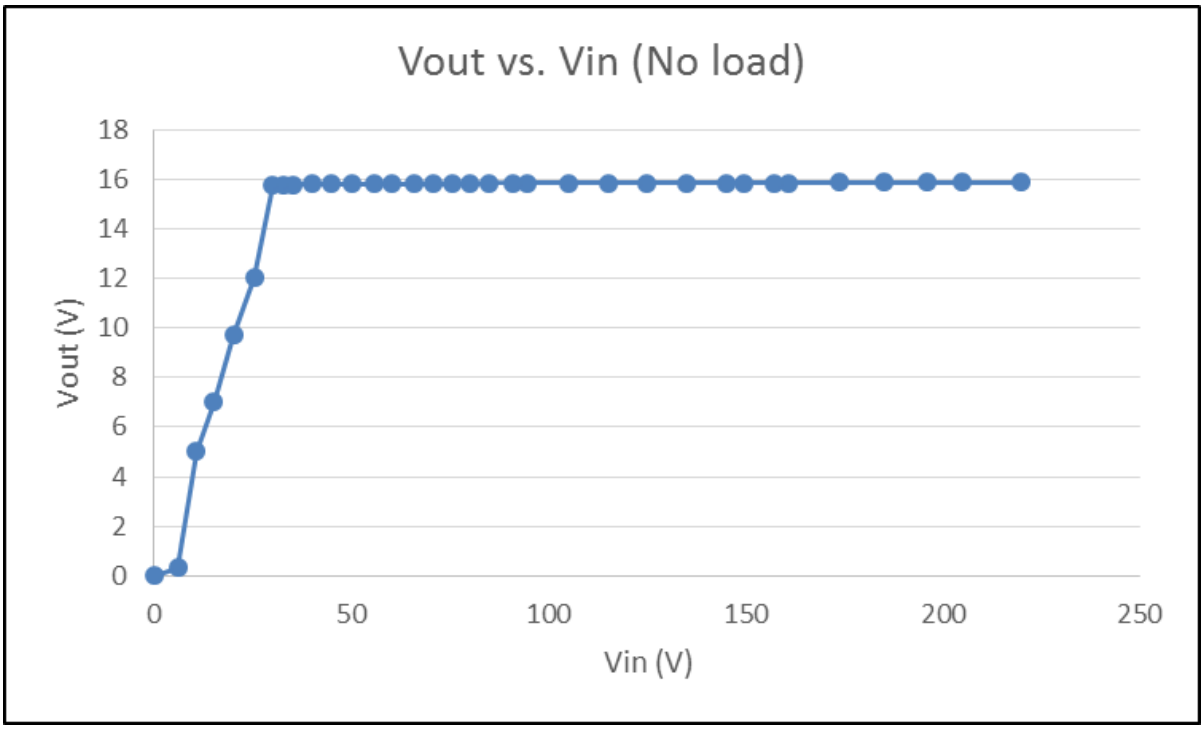

Figure 16: Voltage sweep of flyback converter (No load)

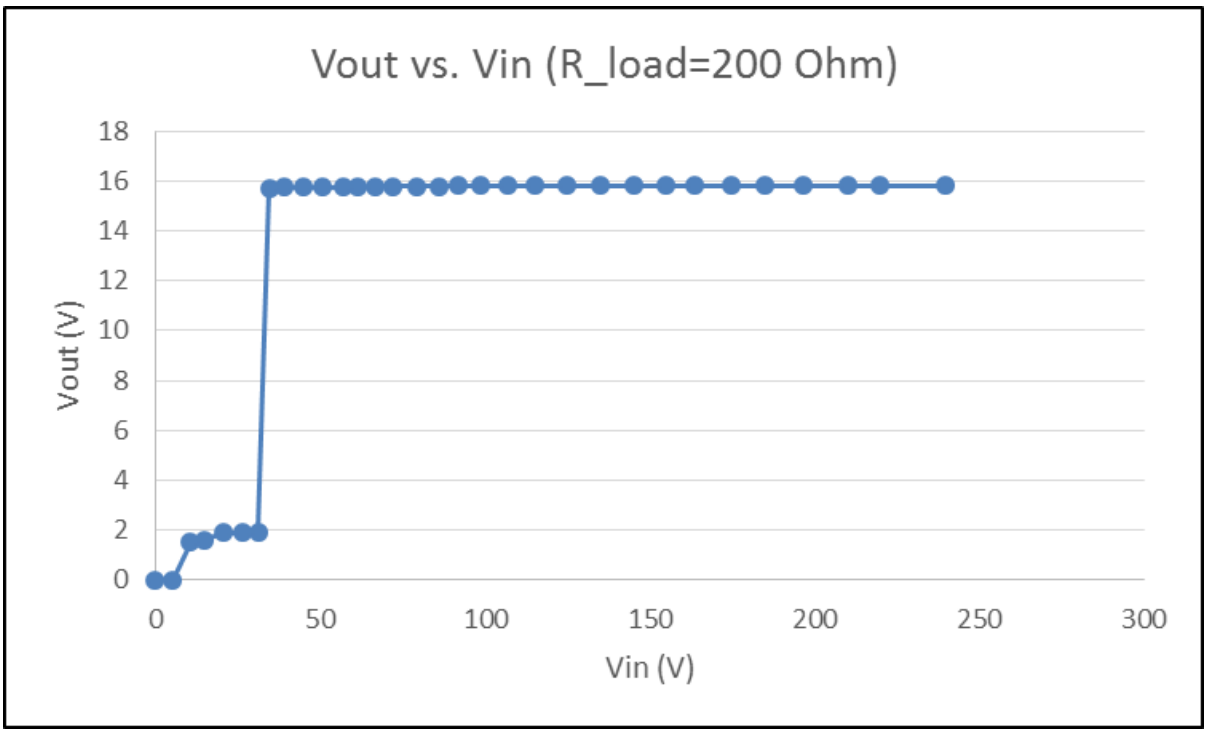

Figure 17: Voltage sweep of flyback converter (R_{load} = 200 Ω)

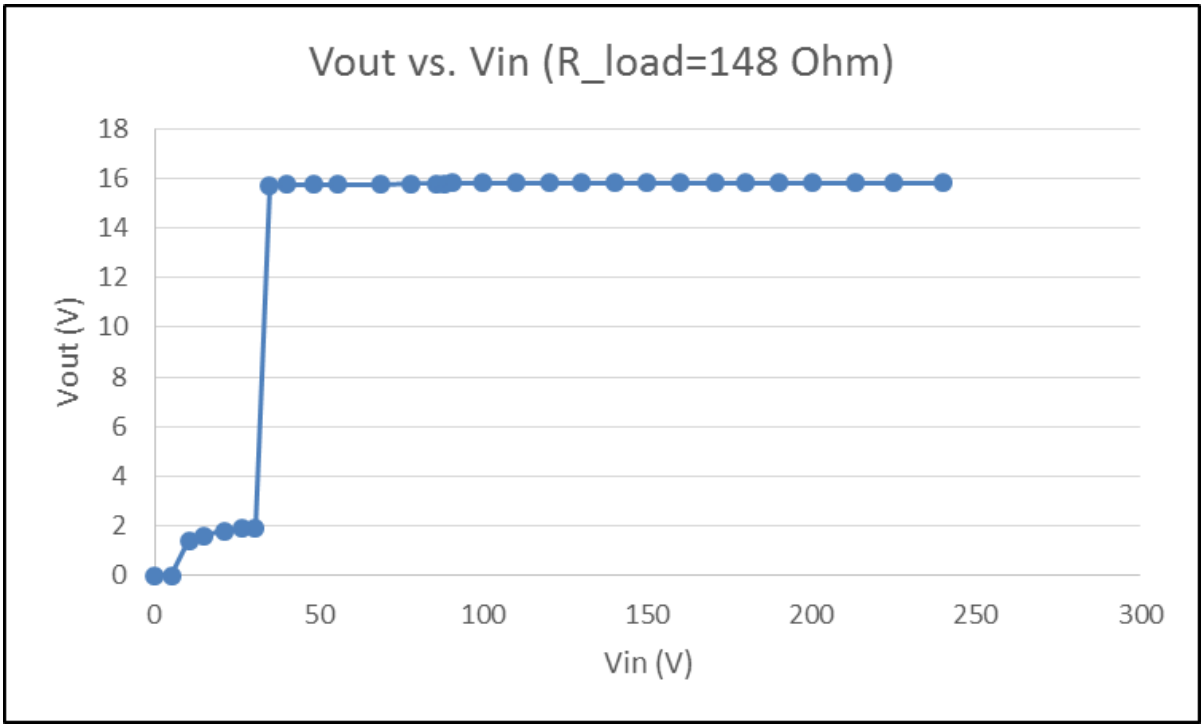

Figure 18: Voltage sweep of flyback converter (R_{load} = 148 Ω)

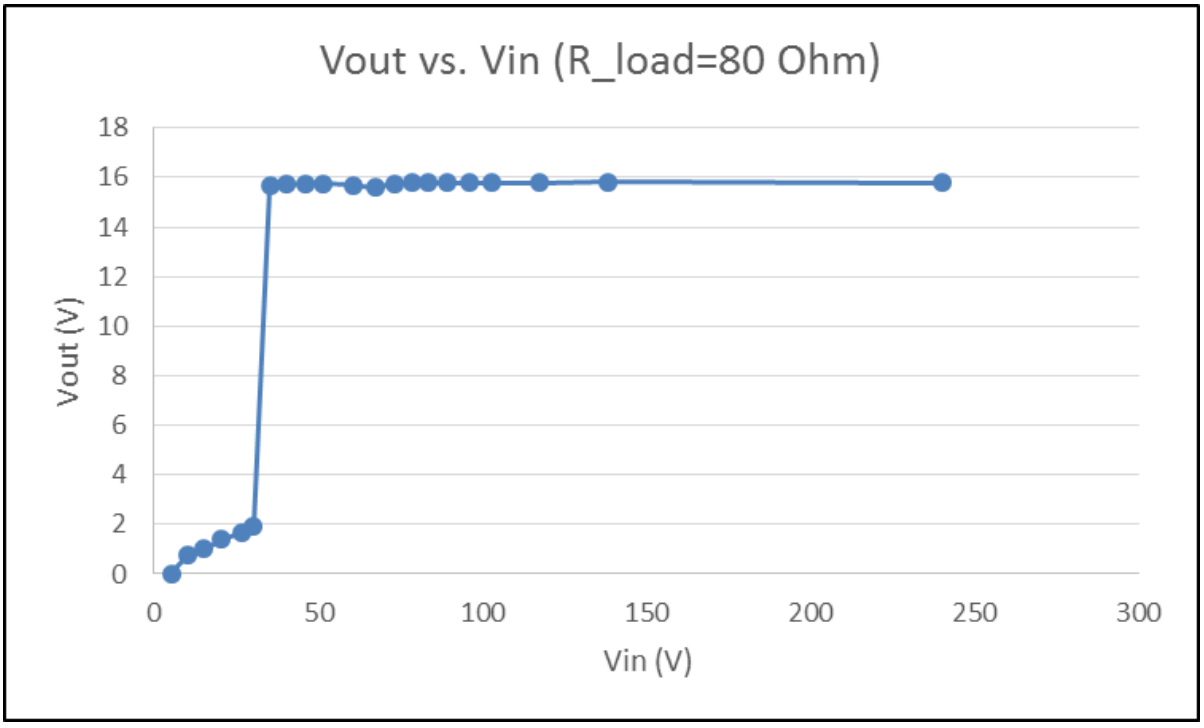

Figure 19: Voltage sweep of flyback converter (R_{load} = 80 Ω)

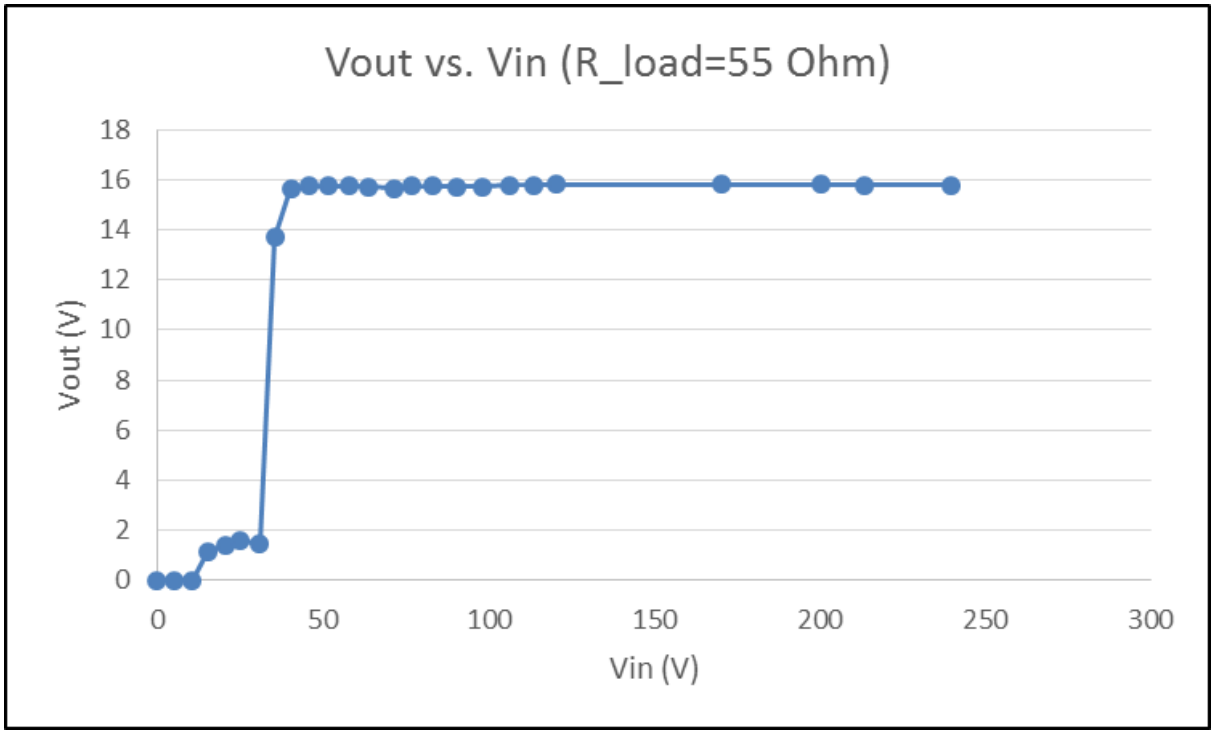

Figure 20: Voltage sweep of flyback converter (R_{load} = 55 Ω)

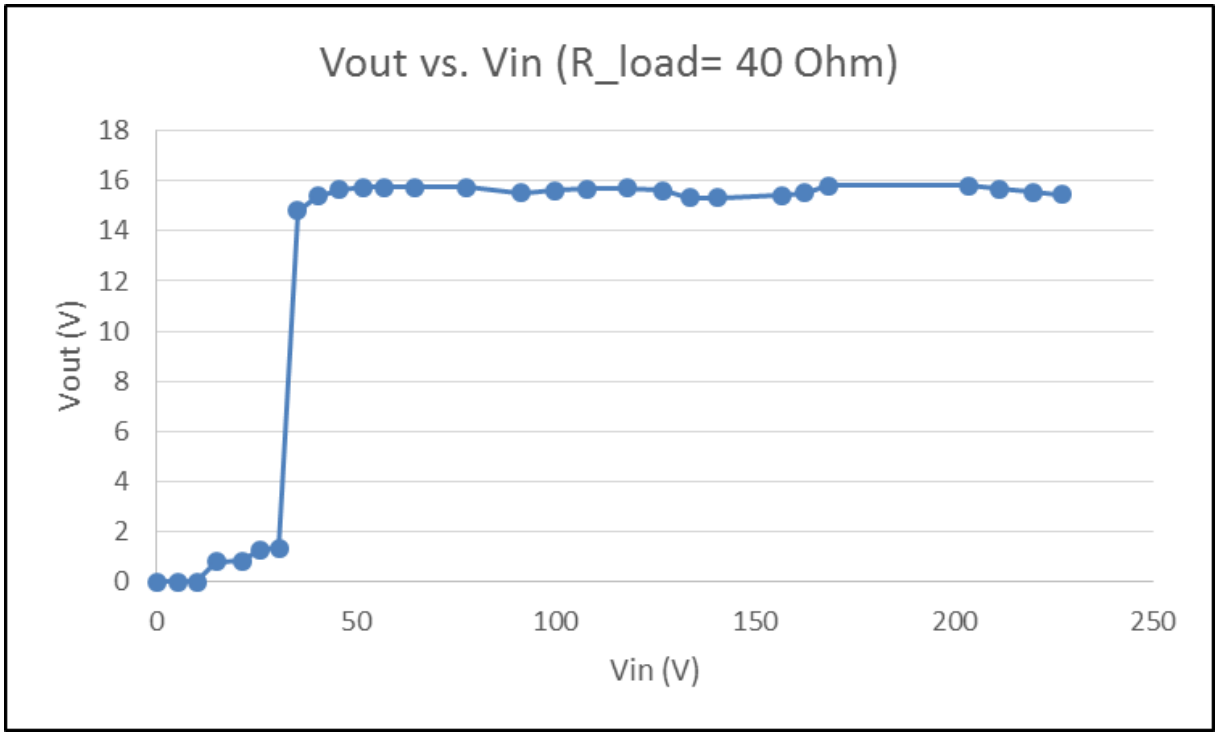

Figure 21: Voltage sweep of flyback converter (R_{load} = 40 Ω)

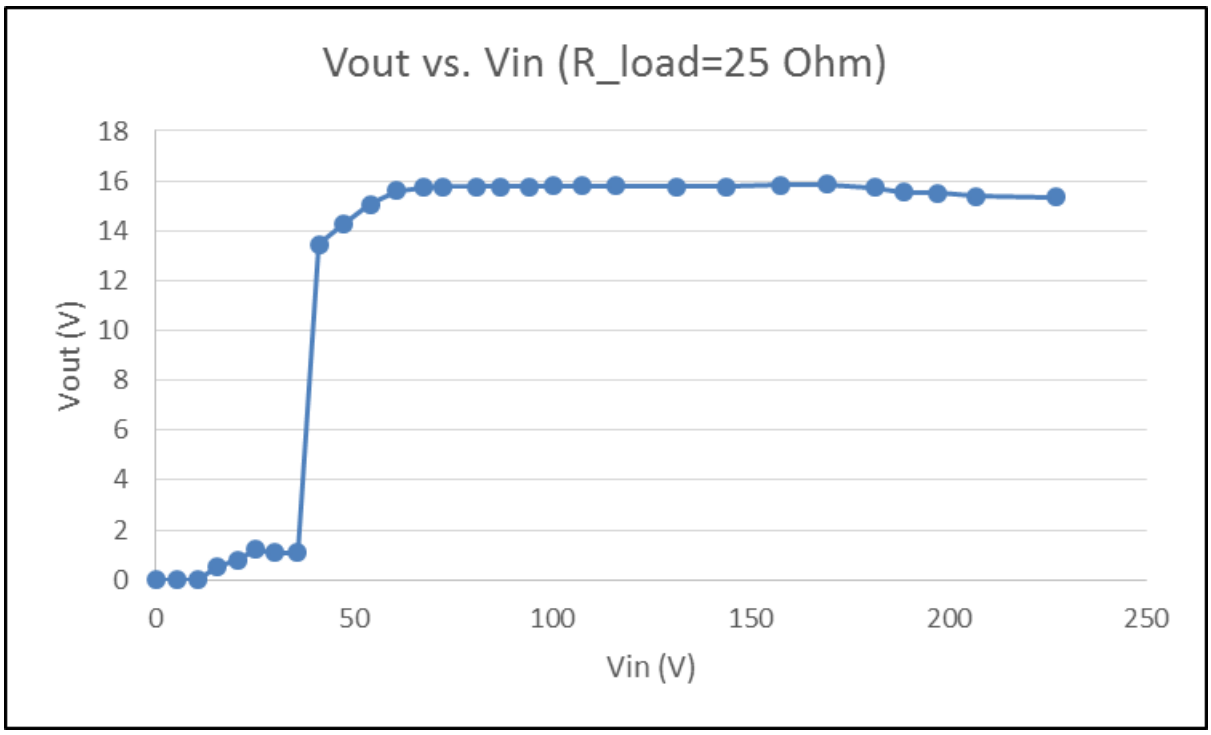

Figure 22: Voltage sweep of flyback converter (R_{load} = 25 Ω)

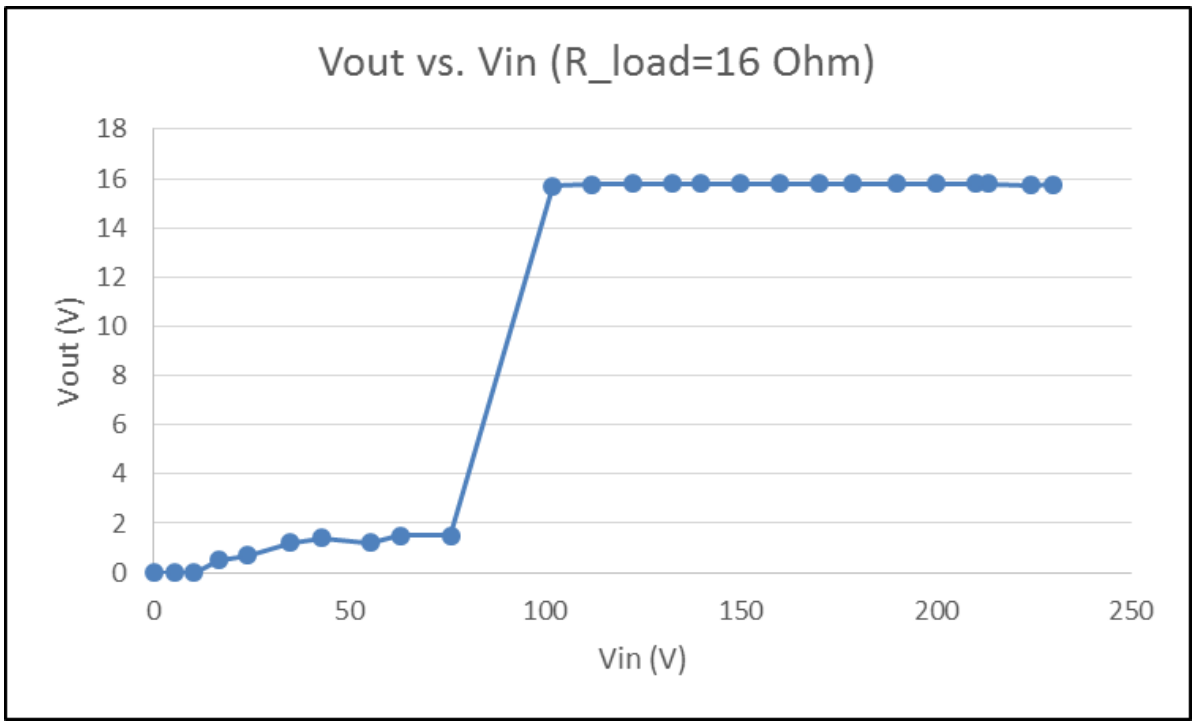

Figure 23: Voltage sweep of flyback converter (Rload = 16 Ω)

2.9 Application

Flyback converter, in this section, was designed for the purpose of driving IGBT gate from output of module capacitor voltage in Modular Multilevel Converter (MMC). A MMC is a

power electronic device which can generate as many level of output voltage as the number of modules in one leg. Functional diagram of a three phase MMC is illustrated in Figure 24.

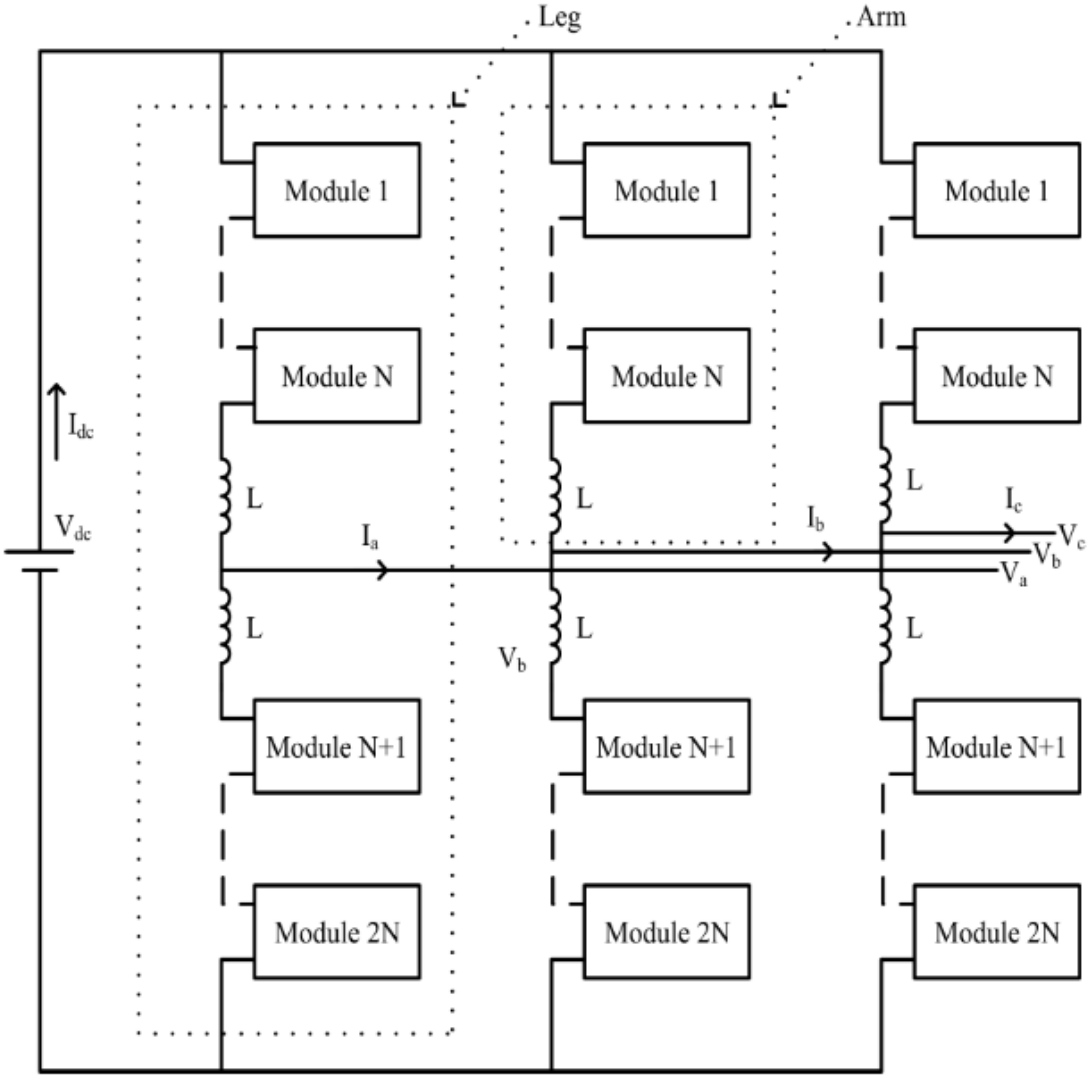

Figure 24: Three phase Modular Multilevel Converter (*Source: Modular Multilevel Converter, Modulation and Control, Sreejith M.R.*)

2.9.1 Pre-charging of module capacitors

One of the challenge associated with MMC is that of pre-charging its module capacitors. Use of auxiliary power supply makes the process cumbersome and expensive. Therefore, active research is undergoing in an attempt to pre-charge module capacitor from main power supply itself. It is achieved in two stage: in the beginning, an uncontrolled pre-charging of module capacitors is initiated through diodes of MOSFET present in series with capacitor (ref. Figure 25 and Figure 26). After a certain threshold voltage is achieved, flyback converters attached at the output of module capacitors are employed for controlled pre-charging using sorting algorithm. Flyback converter was chosen for this low power application because of its requirement for less no. of components.

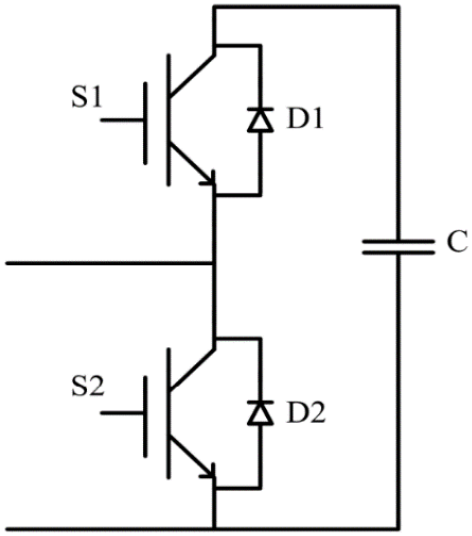

Figure 25: Half bridge cell of a MMC (*Source: Modular Multilevel Converter, Modulation and Control, Sreejith M.R.*)

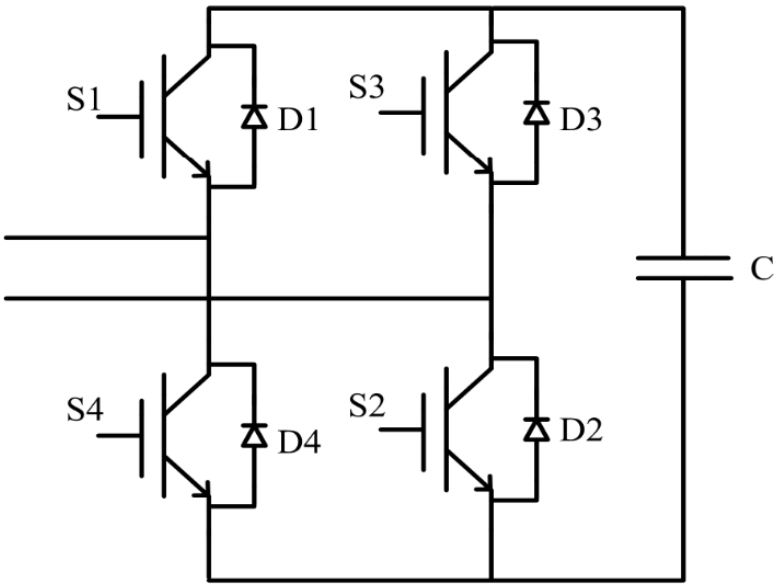

Figure 26: Full bridge cell of a MMC (Source: Modular Multilevel Converter, Modulation and Control, Sreejith M.R.)

The problem with abovementioned technique for controlling gate drives is unstable voltage imbalance across module output due to negative resistance characteristics of flyback converter. Say, a small voltage imbalance of ΔV takes place across module 1 and module 2 of limb 1. This creates a voltage $V + \Delta V$ and $V - \Delta V$ at the output of module 1 and module 2 respectively. Because of this small perturbation, more current will be drawn by flyback converter from module 1 (negative resistance characteristics of flyback converter) and lesser current will be drawn from module 2. This leads to further deterioration of voltage difference.

One way to circumnavigate the problem is by producing unregulated output in the range of 30-40 V from flyback converter followed by a linear regulator such as 7815. Section 2.9.2 discusses two possible types of modification in the existing flyback converter for accommodating this feature.

2.9.2 Design modification

A crude way to generate desired deregulation at output is to add a P-MOSFET in series with TNY279 switch and an N-MOSFET in parallel to this configuration as shown in Figure 27. Reverse breakdown voltage of feedback zener diode (ZD1) is increased to 35 V. During starting phase, P-MOSFET (Q1) remains ON providing a path for TNY279 to bring up the output voltage to 35 V. An external logic immediately turns off the P-MOSFET at this instant and the N-MOSFET (Q2) starts to regulate output voltage in the range of 30 – 40 V using hysteresis control. Logics for MOSFET Q1 and Q2 are not shown in figure for the sake of clarity.

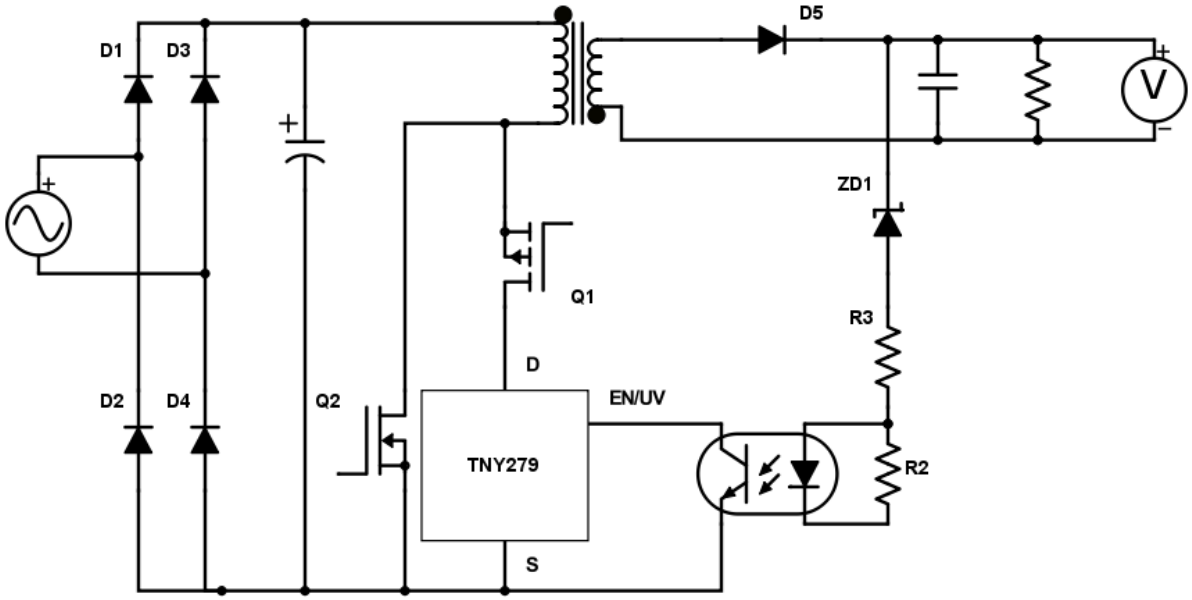

Figure 27: Modified version 1 of flyback converter feedback control

The only drawback of this technique is increase in the number of components leading to high cost of setup.

A second technique is proposed herein which eliminates the need of a P-MOSFET, a major contributor to the total cost of previous setup. BP/M pin of TNY279 IC which provides the utility of overvoltage protection is exploited here. When the required output of 35 V is achieved, BP/M is shorted to pin S by use of an external N-MOSFET, thereby, shutting down the IC. From then on, an external logic based on output voltage feedback, roughly regulates the output in the range of 30 – 40 V. Although total number of components for the setup remains the same, total cost reduces significantly because of replacement of P-MOSFET with N-MOSFET which is lot cheaper. Figure 28 illustrates the schematic of second idea.

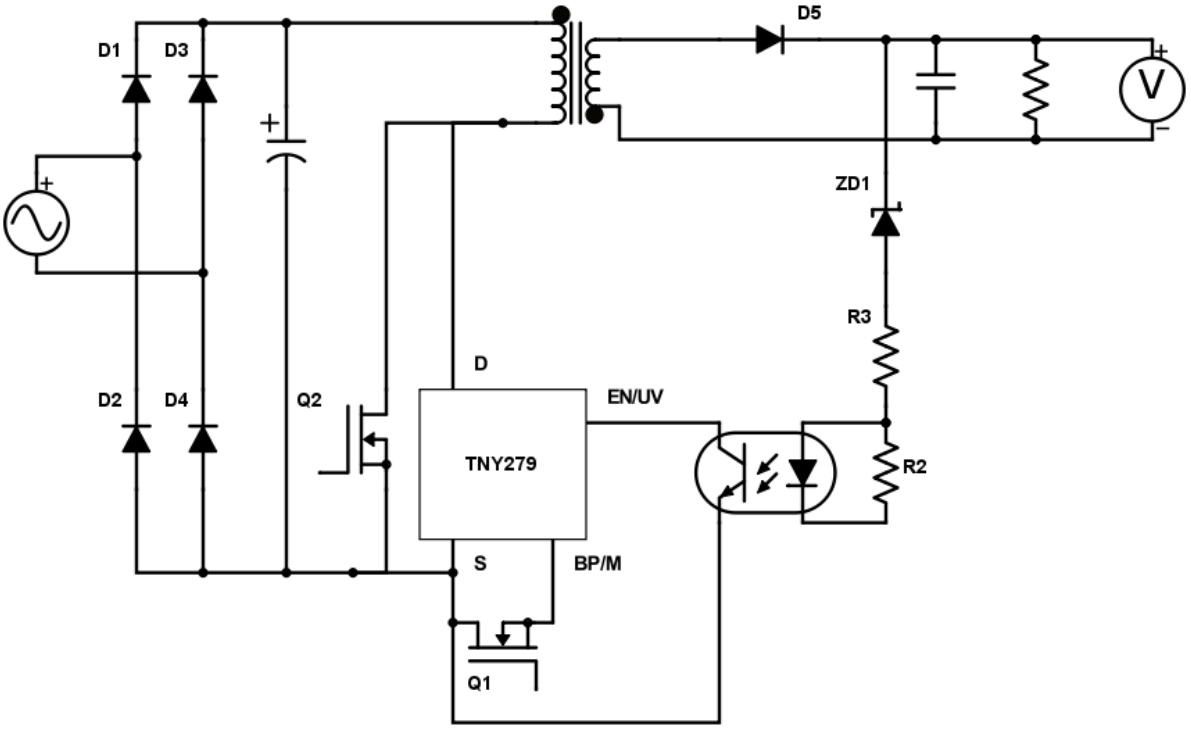

Figure 28: Modification version 2 of flyback converter feedback control

2.9.3 Challenges

Although design modifications in previous subsection eliminates the problem of instability, it is inefficient due to use of linear regulator for high power application. Therefore, steps are being undertaken to utilize a modified version of sorting algorithm for control.

3 Flyback converter for powering Nixie tubes

3.1 Nixie tubes

A nixie tube, or cold cathode display, is an electronic device for displaying numerals or other information using glow discharge. It operates on $180\ V, 0.001 - 0.002\ A$ input power source. Here, in this section, we will design various dc-dc converter for powering nixie tube and discuss their advantages and disadvantages.

3.2 Rating

V_{in}: $180\ V$
I_{in}: $2\ mA$

3.3 Multi-output flyback converter

3.3.1 Motivation

A flyback converter with multi-output terminals is proposed which takes input from 220 VAC power supply and generates output of 180 V and 5 V at its two output terminal. 180 V is used to power nixie tube whereas 5 V supplies power to micro-controller. In order to regulate output, 5 V output terminal is fed back to control circuit as nixie tubes are more tolerable to ripples in voltage than micro-controller. Figure 29 represents the topology for multi-output flyback converter.

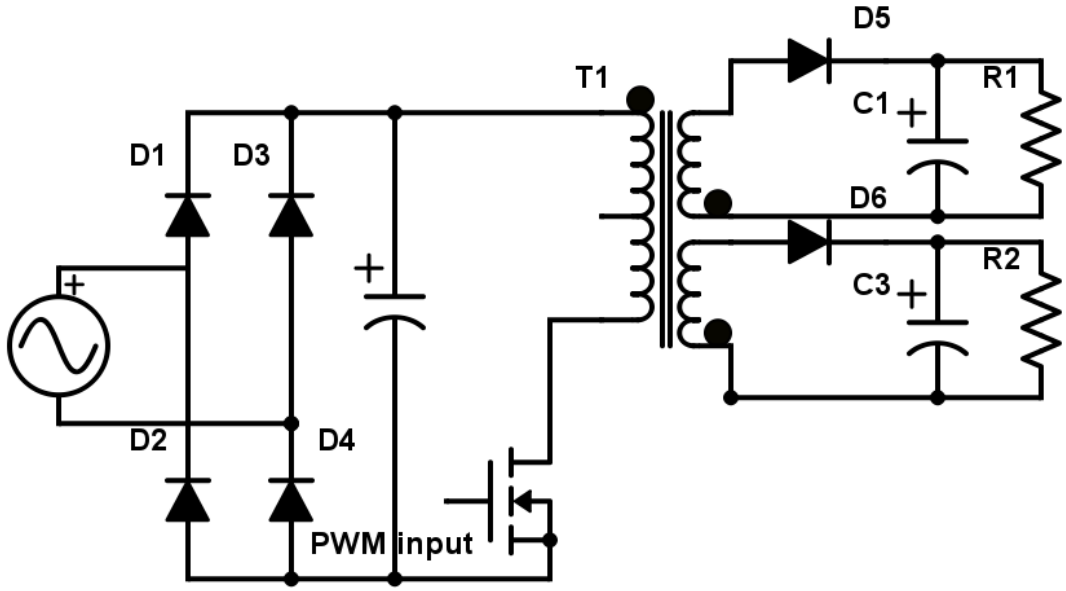

Figure 29: Multi-output flyback converter

3.3.2 Design specification

V_{in}: $220\ VAC$

V_{out_1}: $180\ V, 2\ mA\ (secondary\ winding)$

V_{out_2}: $5\ V, 2\ A\ (tertiary\ winding)$

f_s: 100 kHz

3.3.2.1 Continuous conduction mode

To begin with the design of flyback converter let's assume N1 : N2 = 320 : 181 (because capacitor voltage on primary side of transformer = $220 * \sqrt{2} = 320$ and we have assumed 1 V diode drop on secondary side), N1 : N3 = 320 : 6 and D = 0.5 as a rule of thumb for CCM. Peak value of secondary current comes out to be 0.008 A (refer waveform in Figure 30) using law of energy conservation for one cycle,

$$P_{out}(transformer) = P(diode) + P(load)$$
$$\Rightarrow (V_{out} + 1) * \frac{I_{s_{peak}}}{2} * (1 - D) = V_D * \frac{I_{s_{peak}}}{2} * (1 - D) + V_{out} * I_{out}$$
$$\Rightarrow 181 * \frac{I_{s_{peak}}}{2} * 0.5 = 1 * \frac{I_{s_{peak}}}{2} * 0.5 + 180 * 0.002$$
$$\Rightarrow I_{s_{peak}} = 0.008\ A$$

Let us consider 10 % current ripple in magnetizing inductance. From this we can obtain that value of inductance reflected on secondary side of transformer,

$$\frac{V_{out} + 1}{L} * (1 - D) * T = \frac{10}{100} * 0.008$$
$$\Rightarrow L = 1.13\ H$$

1.13 H of inductance will make the size of converter bulky, hence, we cannot proceed with our design in CCM.

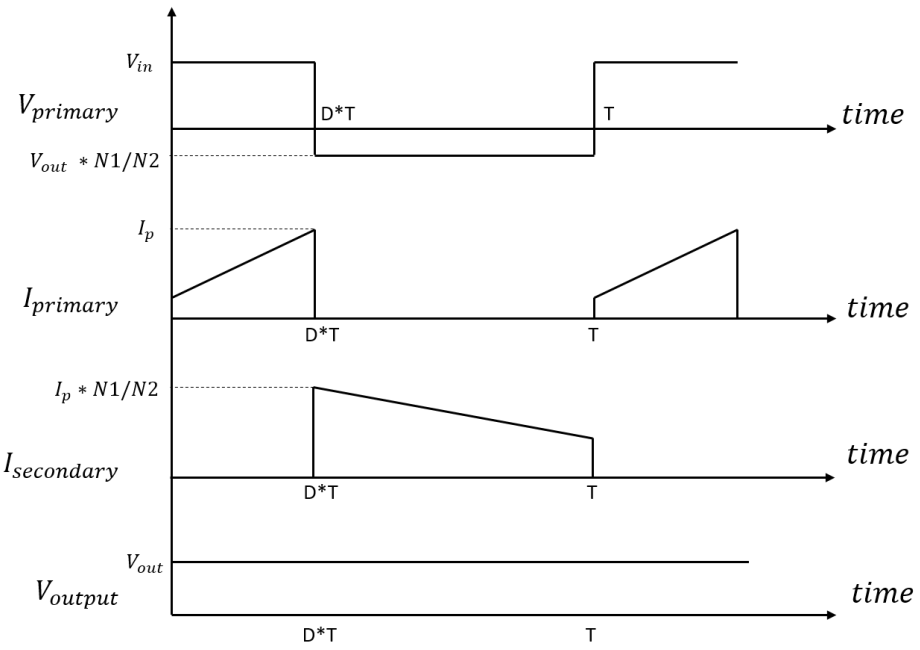

Figure 30: Voltage and current waveform for flyback converter in CCM

3.3.2.2 Discontinuous conduction mode

Given the infeasible value of magnetizing inductance obtained in CCM, let's start with 1 mH as suitable value for magnetizing inductance in DCM. Assuming, as before, turn ratio $N_1 : N_2 =$

$320:181$ and $N_1:N_3 = 320:6$ (keeping in mind 1 V drop across output diode). From equation $V = L\frac{di}{dt}$ we obtain,

$$\frac{V_p}{L_p} * D * T = Ip_{peak}$$

$V_p : Primary\ side\ voltage$

$L_p : Magnetizing\ inductance\ on\ primary\ side$

$Ip_{peak} : Peak\ value\ of\ primary\ current$

$D : Duty\ cycle$

And from law of conservation of energy we get,

$$V_p * \frac{Ip_{peak}}{2} * D = 181 * 0.002 + 6 * 2$$

Dividing above two equations we obtain value of peak secondary current,

$$Ip_{peak} \approx 0.5\ A$$

Substituting Ip_{peak} in any of the two equations we get,

$$D = 0.15625$$

Note that obtained value of duty cycle is applicable for full load condition only. Therefore, a closed loop control is mandatory for variable load. Figure 31 represents typical waveforms for DCM operation at steady state. Similarly, capacitance values can be obtained by satisfying the specification of 1% ripple in voltage.

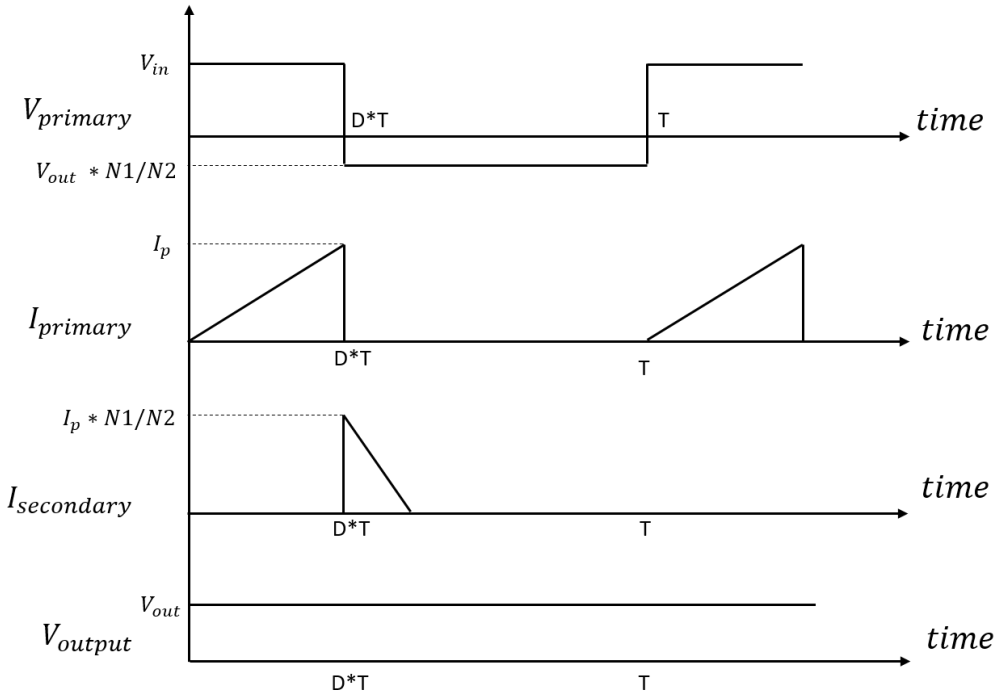

Figure 31: Voltage and current waveform for flyback converter in DCM

3.3.3 Transformer design

Now that basic parameters for the design have been derived, we can focus on the design of transformer. One of the popular method in literature for the design of high frequency transformer is area product approach. We will use the same procedure for our design. We know that

$$V_1 = N_1 * \frac{d\phi}{dt} \approx N_1 * \frac{\Delta B * A_c}{D * T}$$

$$\Rightarrow N_1 = V_{1_{max}} * \frac{D * T}{\Delta \mathrm{B} * \mathrm{A_c}}$$

$\Delta B: Change\ in\ flux\ density\ (0.3\ T\ for\ high\ frequency\ core)$

Similarly,

$$N_2 = V_{2_{max}} * \frac{D_1 * T}{\Delta B * A_c}$$

$$N_3 = V_{3_{max}} * \frac{D_1 * T}{\Delta B * A_c}$$

$D_1: Fraction\ of\ a\ cycle\ for\ which\ output\ diode\ is\ in\ conducting\ mode$

In order to get a successful design, our windings should fit in the given window area.

$$i.e. K_w * A_w = N_1 * a_1 + N_2 * a_2 + N_3 * a_3 = N_1 * \frac{I_1}{J} + N_2 * \frac{I_2}{J} + N_3 * \frac{I_3}{J}$$

$K_w: packing\ factor\ (0.4\ for\ transformer\ design)$

$I_1: R.M.S.\ value\ of\ primary\ current$

$I_2: R.M.S.\ value\ of\ secondary\ current$

$I_3: R.M.S.\ value\ of\ tertiary\ current$

$J: Current\ density\ (3\ A/mm^2)$

$A_w: Window\ area\ of\ core$

Substituting value of N_1, N_2 and N_3 from previous equation, we get

$$K_w * A_w * J * \Delta B * A_c * f_s = V_{1_{max}} * D * I_1 + V_{2_{max}} * D_1 * I_2 + V_{3_{max}} * D_1 * I_3$$

Divide and multiply R.H.S. with average current of each term

$$\Rightarrow K_w * A_w * J * \Delta B * A_c * f_s$$
$$= V_{1_{max}} * D * \frac{I_{1_{avg}} * I_1}{I_{1_{avg}}} + V_{2_{max}} * D_1 * \frac{I_{2_{avg}} * I_2}{I_{2_{avg}}} + V_{3_{max}} * D_1 * \frac{I_{3_{avg}} * I_3}{I_{3_{avg}}}$$

$$\Rightarrow K_w * A_p * J * \Delta B * f_S = P_{o1} * \frac{I_1}{I_{1_{avg}}} + P_{o2} * \frac{I_2}{I_{2_{avg}}} + P_{o3} * \frac{I_3}{I_{3_{avg}}}$$

$A_p: Area\ product\ (A_c * A_w)$

$P_{oi}: Average\ power\ output\ (\forall\ i = 1, 2, 3)$

For DCM operation mode, we can substitute the value on RHS to obtain

$$K_w * A_p * J * \Delta B * f_s = (P_{o2} + P_{o3})\left(\frac{1}{\eta} * \sqrt{\frac{4 * D}{3}} + \sqrt{\frac{4 * (1 - D)}{3}}\right)$$

$\eta: efficiency\ of\ converter\ (\approx 90\ \%)$

$$\frac{I_{rms}}{I_{avg}} = \sqrt{\frac{4 * D}{3}}\ for\ DCM\ operation$$

On substituting values in equation above, we get $A_p = 538\ mm^4$. Standard table for magnetic characteristics of ferrite core recommends use of EE20/10/5 core with $A_p = 1490\ mm^4, A_w = 47.8\ mm^2, A_c = 31\ mm^2$. Now, we need to calculate R.M.S. values for current waveforms.

$$I_1 = \frac{1}{T}\sqrt{\int_0^{DT}\left(\frac{V_{in}}{L_p} * t\right)^2} = 0.117\ A$$

$$I_2 = \frac{N_1}{N_2} * I_1 = 0.207\ A$$

$$I_3 = \frac{N_1}{N_3} * I_1 = 6.24$$

Using R.M.S. value obtained in previous step, we can re-verify that our winding fits in the window area.

$$i.e. N_1 * \frac{I_1}{J} + N_2 * \frac{I_2}{J} + N_3 * \frac{I_3}{J} \leq K_w * A_w = 0.4 * 47.8 = 19.12$$

$$N_1 = V_{1_{max}} * \frac{D * T}{\Delta \mathrm{B} * \mathrm{A_c}} = \frac{320 * 0.16525 * 10^{-5}}{0.3 * 31 * 10^{-6}} \approx 57$$

$$N_2 = \frac{181}{320} * 57 \approx 32$$

$$N_3 = \frac{6}{181} * 32 \approx 1$$

$$\therefore 57 * \frac{0.117}{3} + 32 * \frac{0.207}{3} + 1 * \frac{6.24}{3} = 10.927$$

As $10.927 < 19.12$, winding will comfortably fit into available window area. We now need to find air gap required to achieve required inductance using

$$l_g = \mu_0 * N^2 * \frac{A_c}{L_p}$$

$$\Rightarrow l_g = 0.12\ mm$$

$l_g: Air\ gap\ length$

The last step is to find standard wire gauge for each winding and then the design process is complete.

$$a_1 = \frac{I_1}{3} = 0.039\ mm^2 \therefore SWG = 34$$

$$a_2 = \frac{I_2}{3} = 0.069\ mm^2 \therefore SWG = 31$$

$$a_3 = \frac{I_3}{3} = 2.08\ mm^2 \therefore SWG = 15$$

3.3.4 Results

Flyback converter designed in this section was simulated for full load in Simulink. Figure 32 depicts the Simulink model for the multi-output flyback converter. Rectified 220 VAC input was fed to the input of converter and a closed loop control was implemented using PI controller block with 5 V as the reference voltage. Parameters K_p and K_I were set to 1 and 15 respectively after successive trial and error method. Output error was given to a PWM generator block for generating switching pulses for MOSFET. Resulting voltage waveforms for two output terminals are shown in Figure 33 and Figure 34 and input current waveform at steady state is shown in Figure 35. Peak value of 5 A input current during steady state indicates that our design was correct.

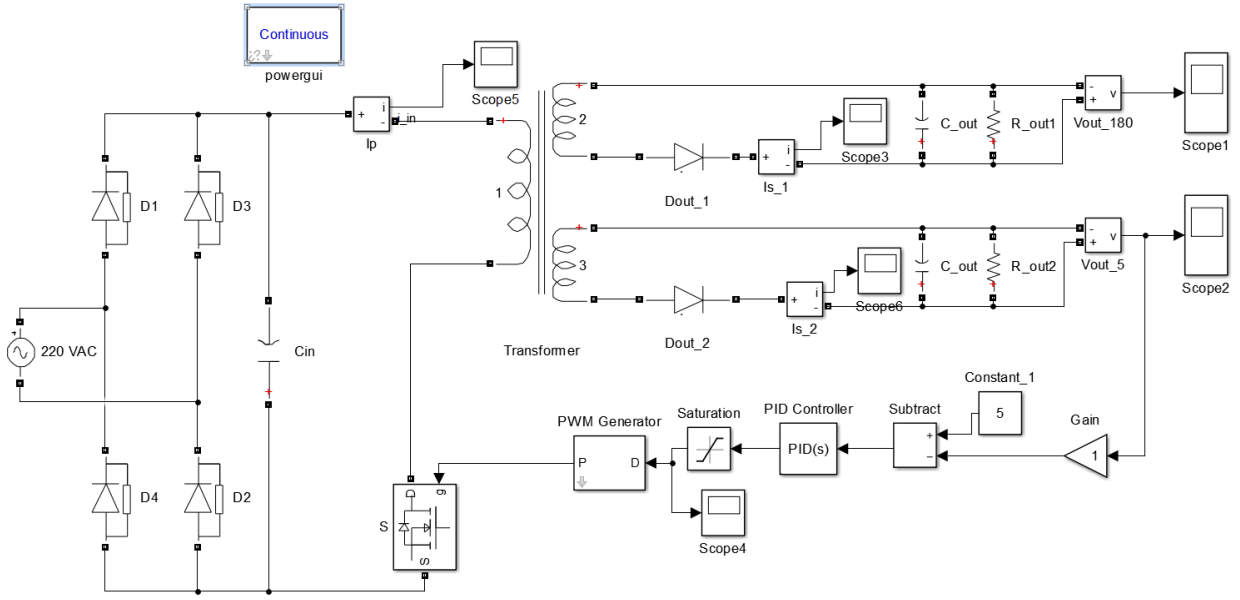

Figure 32: Simulink model for multi-output closed-loop flyback converter

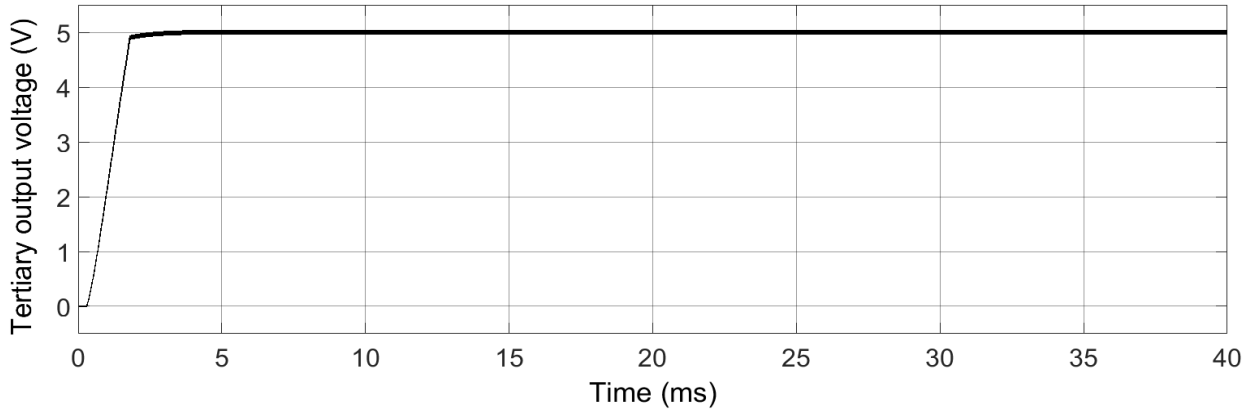

Figure 33: Simulation waveform for 5 V output terminal

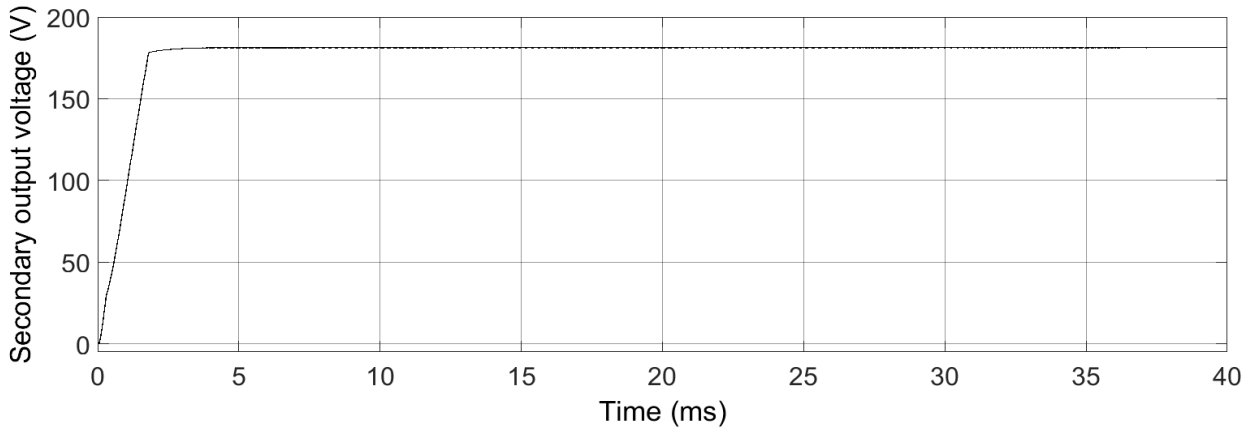

Figure 34: Simulation waveform for 180 V output terminal

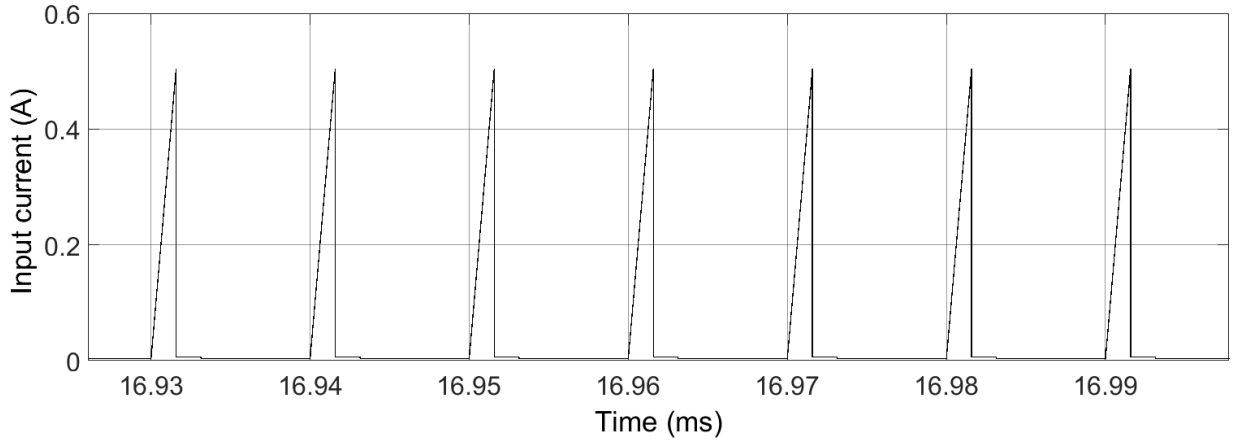

Figure 35: Input current waveform for DCM operation at steady state

3.4 USB powered flyback converter

In the early part of this project, idea of using USB port (5 V, 0.5 A power supply) to power nixie tube was proposed using multi stage converter. If we were to use a single stage boost converter, it would require 97.2 % duty cycle (D) for its steady state operation. Practically it is not advisable to go beyond 90 % duty cycle, hence, a multi-stage design using boost converter was proposed. It consisted of two cascaded boost converter: first stage boosts the input voltage from 5 V to 30 V followed by second stage which boosts it to 180 V. It had its own

demerits in terms of high input current and absence of galvanic isolation between its input and output. Further, operation in continuous mode required large inductance value. In order to tackle these problem, a flyback converter design operating is proposed. Again the problem of high inductance value exists if we were to operate in CCM, so, operational design in DCM is made in following section. Added advantage of powering

3.4.1 Design

Based on the design principle followed in Section 3.3.2.2, we can apply law of energy conservation to obtain,

$$V_p * V_p * \frac{D}{2 * L_p} * D = 181 * 0.002$$
$$\Rightarrow D^2 = L_p * 2896$$

To obtain L_p, use the maximum input current limitation. Let's keep $I_{p_{peak}} = 0.3\ A$ to be on safer side i.e. to avoid current overshoot to exceed 0.5 A during transient. More on this will be discussed in results section. Therefore,

$$\frac{V_p}{L_p} * D * T = 0.3$$
$$\Rightarrow D = 6000 * L_p$$

Dividing above two equations, we obtain

$$D = \frac{2896}{6000} = 0.483\ and\ L_p = 80.5\ \mu H$$

3.4.2 Transformer design

Refer to Section 3.3.3 for detailed derivation of transformer design. We can use the result obtained to get area product for transformer using

$$K_w * A_p * J * \Delta B * f_s = P_{o2} * \left(\frac{1}{\eta} * \sqrt{\frac{4 * D}{3}} + \sqrt{\frac{4 * (1 - D)}{3}} \right)$$
$$\Rightarrow A_p = \frac{0.623}{36000} = 17.3\ mm^4$$

Standard table for magnetic characteristics of ferrite core recommends use of EE20/10/5 core with $A_p = 1490\ mm^4, A_w = 47.8\ mm^2, A_c = 31\ mm^2$. Now, we need to calculate R.M.S. values for current waveforms.

$$I_1 = \frac{1}{T} \sqrt{\int_0^{DT} \left(\frac{V_{in}}{L_p} * t \right)^2} = 0.21\ A$$

$$I_2 = \frac{N_1}{N_2} * I_1 = 5.81\ mA$$

Using R.M.S. value obtained in previous step, we can re-verify that our winding fits in the window area.

$$i.e. N_1 * \frac{I_1}{J} + N_2 * \frac{I_2}{J} + N_3 * \frac{I_3}{J} \leq K_w * A_w = 0.4 * 47.8 = 19.12$$

$$N_1 = V_{1_{max}} * \frac{D * T}{\Delta B * A_c} = \frac{5 * 0.483 * 10^{-5}}{0.3 * 31 * 10^{-6}} \approx 3$$

$$N_2 = \frac{181}{5} * 3 \approx 109$$

$$\therefore 3 * \frac{0.21}{3} + 109 * \frac{0.00581}{3} = .421$$

As $0.421 < 19.12$, winding will comfortably fit into available window area. We now need to calculated air gap required to achieve given inductance using

$$l_g = \mu_0 * N^2 * \frac{A_c}{L_p}$$
$$\Rightarrow l_g = 4.35 * 10^{-3}\ mm$$

l_g: $Air\ gap\ length$

The last step is to find standard wire gauge for each winding and then the design process is complete.

$$a_1 = \frac{I_1}{3} = 0.07\ mm^2 \therefore SWG = 30$$

$$a_2 = \frac{I_2}{3} = 0.00194\ mm^2 \therefore SWG = 45$$

3.4.3 Results

Flyback converter designed was simulated for full load in Simulink. Figure 36 depicts the Simulink model for the designed flyback converter. 5 V input was fed from a dc source and a closed loop control was implemented using PI controller block parameters K_p and K_I set to .0001 and 0.1 respectively after successive trial and error method. Output error was given to a PWM generator block for generating switching pulses for MOSFET. Small value of K_p was chosen to avoid large input current overshoot as output capacitor is uncharged at start. Plot of output voltage and input current are shown in Figure 38 and Figure 40 respectively. With chosen parameter values for PID block, input current is always less than maximum current rating of USB port. Recapitulate that initial current is due to uncharged output capacitor which causes secondary current even in the ON state of switch.

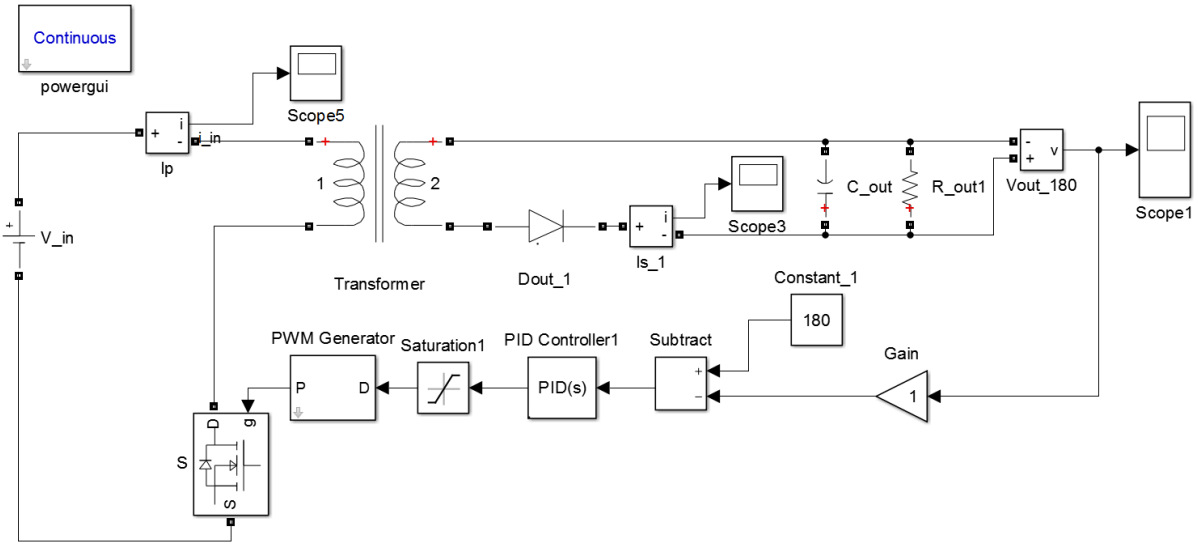

Figure 36: Simulink model of the closed-loop flyback converter

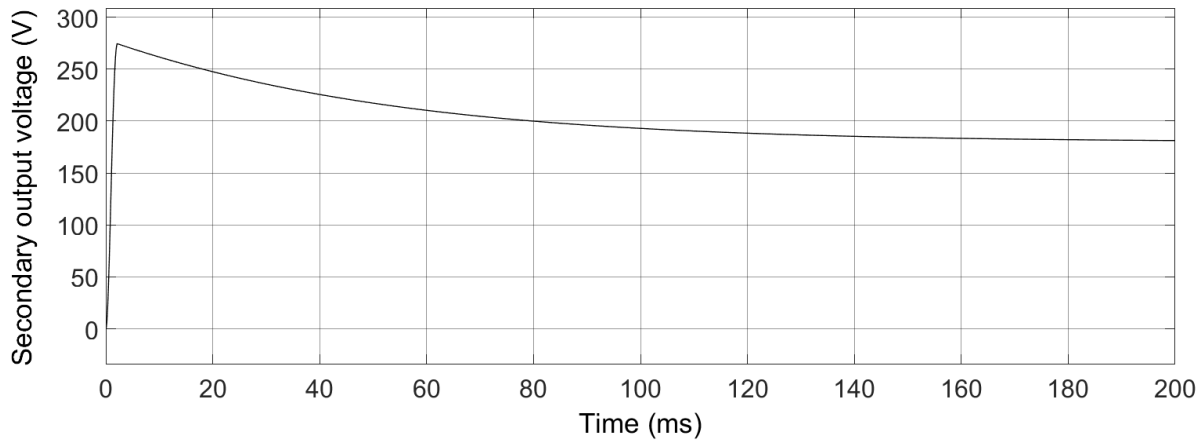

Figure 37: Output voltage waveform of the open loop flyback converter

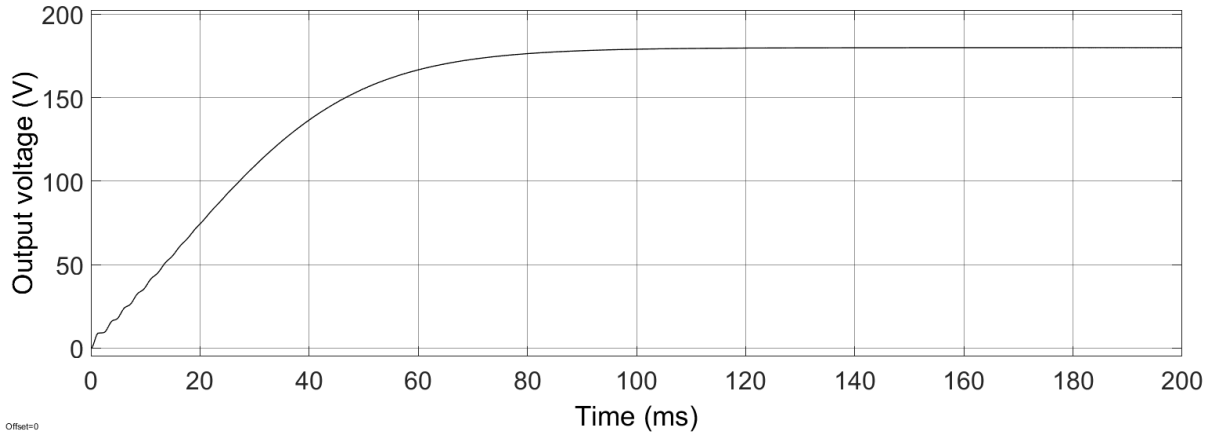

Figure 38: Output voltage waveform of the closed-loop flyback converter

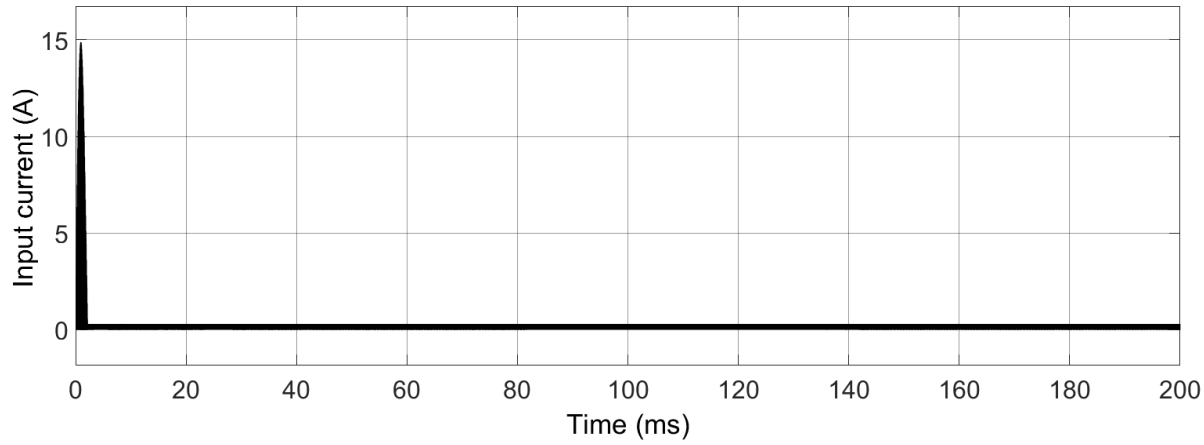

Figure 39: Input current waveform the closed loop flyback converter

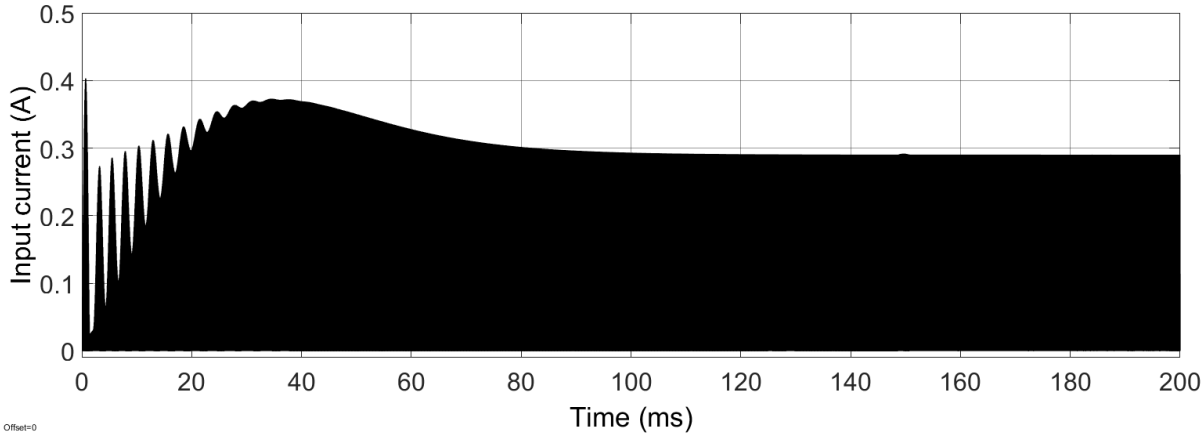

Figure 40: Input current waveform of the closed-loop flyback converter

3.5 Conclusion

For dc-dc converter with low output power requirement, as was in our case of Nixie tube power supply, design in continuous conduction mode leads to high inductance value requirement. Hence, it is advisable to design them in discontinuous conduction mode so as to reduce inductance and make the hardware compact and economical. Further, DCM operation results in lower input current requirement allowing use of thin wire for inductor winding. Small input current also leads to increased efficiency of converter.

4 Reference

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